A Case for 3D Stacked Analog Circuits in High Speed Sensing Systems

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1. Introduction

- High speed, low power sensing systems are critical
  - Sensor systems have both digital and analog components
- CMOS scaling improved digital components
  - Less power, area and higher speed
- Analog components (input buffers & amplifiers) negatively impacted:
  - Matching, transconductance and transistor gain reduced
- Better linearity and gain requires BICMOS
- Mixing BICMOS and CMOS on the same die is challenging

| Tech Node | V_{dd} (V) | Gm(S) | Intr
<table>
<thead>
<tr>
<th></th>
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</thead>
<tbody>
<tr>
<td>90nm</td>
<td>0.83</td>
<td>1.63e-4</td>
<td>20</td>
</tr>
<tr>
<td>65nm</td>
<td>0.73</td>
<td>2.00e-4</td>
<td>18</td>
</tr>
<tr>
<td>45nm</td>
<td>0.62</td>
<td>2.62e-4</td>
<td>15</td>
</tr>
<tr>
<td>32nm</td>
<td>0.53</td>
<td>3.47e-4</td>
<td>12</td>
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Table 1: Technology Scaling Trends, L=kmin

2. 3D Stacking

- 3D stacking integrates multiple technology nodes in the vertical dimension
  - Already used to stack memory
- This paper goal:
- Target system used to quantify power and performance benefits of 3D
  - Input buffers receive analog signal and supply it to the ADC.
  - ADC is responsible for converting the analog signal into its digital

3. Three Interface Models: Bond-Wire, Flip Chip, TSV

- Wire bonding and Flip Chip models commonly used today.
- RLC lumped models developed for the three different interface models
- Skin effect is taken into consideration to model the interface behavior at high frequencies

4. System Specifications

- RLC models used to interface blocks of the system under study.
- High performance building blocks have been implemented using the appropriate and most efficient technology nodes.
  - 12 GHz Input buffer implemented in IBM 90nm BICMOS process.
  - Input signal has a 3GHz bandwidth and .3V peak to peak voltage swing.
  - A high speed Sample and Hold (S/H) circuit with the specifications listed in Table 3.

<table>
<thead>
<tr>
<th>Signal Frequency</th>
<th>Sampling Frequency</th>
<th>Sampling Capacitance</th>
<th>Technology</th>
<th>ENOB</th>
<th>Tracking BW</th>
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<tbody>
<tr>
<td>3GHz</td>
<td>10GHz</td>
<td>1pF</td>
<td>45nm</td>
<td>7-bit</td>
<td>&gt;5GHz</td>
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</table>

Table 3: Specifications for S/H Circuit

5. Simulation Results

A. Bandwidth

- Interface bandwidth a determining factor for the input signal frequency
  - Mainly depends on the input impedance seen at the output of the buffer for a given signal frequency.

Input Impedance
- TSV impedance 8X < .5mm bonding wire
- TSV impedance 3X < Flip Chip

Tracking Bandwidth
- TSV
  - 1GHz tracking bandwidth
- Flip Chip
  - 7.8GHz
- Bonding Wire
  - 5.6 GHz

B. Power

- We measured the Input buffer power consumption when integrated with the ADC using different interfaces.
  - TSV power 10X < 1nH bonding wire.
  - TSV power 30% < Flip-chip

C. Signal Integrity

- Two well known metrics: Spurious Free Dynamic Range (SFDR) and signal to noise and distortion ratio (SNDR).
  - Transient noise is taken into consideration during simulations.
  - The large inductance and the lower tracking bandwidth degrade the obtained SNDR when bonding wire interface is used.
- SNDR varies by 4 dB for different values of the bonding wire inductance.
- Flip chip shows a 2.5dB degradation in the SNDR.
- TSV results similar to the no-interface case
- SNDR for the 5um and 2um TSVs is 0.1dB.