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A Case for 3D Stacked Analog Circuits in High Speed Sensing Systems

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1. Introduction

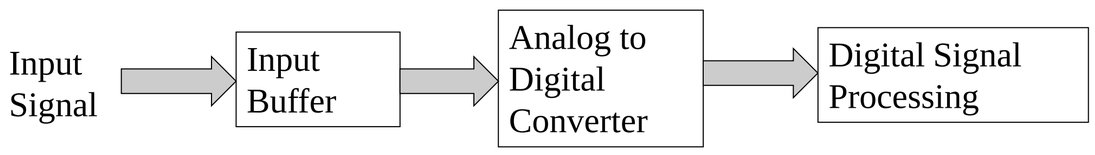
- High speed, low power sensing systems are critical
  - Sensor systems have both digital and analog components
- CMOS scaling improved digital components
  - Less power, area and higher speed
- Analog components (input buffers & amplifiers) negatively impacted:
  - Matching, transconductance and transistor gain reduced
- Better linearity and gain requires BICMOS
- Mixing BICMOS and CMOS on the same die is challenging

Table 1:Technology Scaling Trends, $L=L_{min}$

Tech Node	V_{swing}	Gds(S)	Intrinsic Gain(dB) W/L=10	A_{vt} Match	Max Freq.(GHz)
90nm	0.83	1.63e-4	20	6	170
65nm	0.73	2.00e-4	18	5	240
45nm	0.62	2.62e-4	15	5	320
32nm	0.53	3.47e-4	12	5	400

2. 3D Stacking

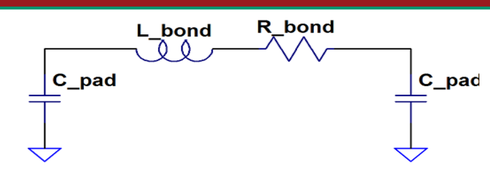
- 3D stacking integrates multiple technology nodes in the vertical dimension
  - Already used to stack memory
- This paper goal:
  - TSV-centric 3D integration of future analog-analog/digital interface systems.
- Target system used to quantify power and performance benefits of 3D
  - Input buffers receive analog signal and supply it to the ADC.
  - ADC is responsible for converting the analog signal into its digital



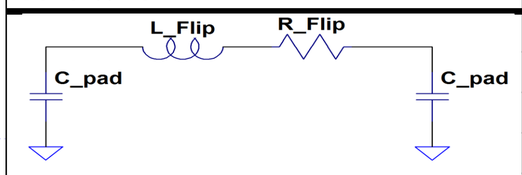
Basic building blocks for data acquisition systems

3. Three Interface Models: Bond-Wire, Flip Chip, TSV

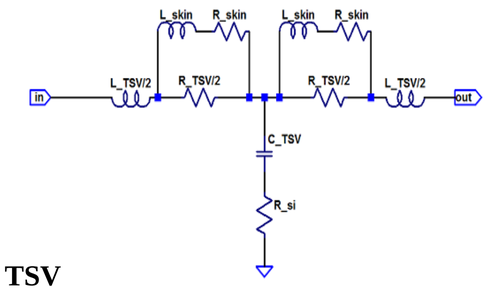
- Wire bonding and Flip Chip models commonly used today.
- RLC lumped models developed for the three different interface models
- Skin effect is taken into consideration to model the interface behaviour at high frequencies.



Bond Wire



Flip Chip



TSV

Diameter	25um
Length	1mm
L_{bond}	1nH
R_{bond}	10mΩ
C_{pad}	100fF
Diameter	25-50um
Length	.1mm
L_{flip}	80pH
R_{flip}	30mΩ
C_{pad}	100fF
Diameter	5um
Length	50um
L_{TSV}	34pH
R_{TSV}	44mΩ
C_{TSV}	200fF
Dielectric thickness	100nm

Table 2: Lumped RLC Models and parameters values

4. System Specifications

- RLC models used to interface blocks of the system under study.
- High performance building blocks have been implemented using the appropriate and most efficient technology nodes.
  - 12 GHz Input buffer implemented in IBM 90nm BICMOS process.
  - Input signal has a 3Ghz bandwidth and .3V peak to peak voltage swing.
  - A high speed Sample and Hold (S/H) circuit with the specifications listed in Table 3.

Table 3: Specifications for S/H Circuit

Signal Frequency	3GHz
Sampling Frequency	10GHz
Sampling Capacitance	4pF
Technology	45nm
ENOB	7-bits
Tracking BW	>5GHz

5. Simulation Results

A. Bandwidth

- Interface bandwidth a determining factor for the input signal frequency
  - Mainly depends on the input impedance seen at the output of the buffer for a given signal frequency.

Input Impedance

- TSV impedance 8X < .5mm bonding wire
- TSV impedance 3X < Flip Chip

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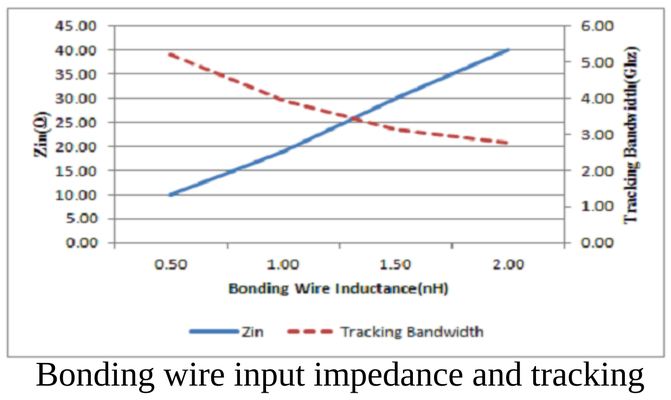
Tracking Bandwidth

- TSV
  - 11Ghz tracking bandwidth.
- Flip Chip
  - 7.8Ghz
- Bonding Wire
  - 5.6 GHz.



Bonding wire input impedance and tracking bandwidth

B. Power

- We measured the Input buffer power consumption when integrated with the ADC using different interfaces.
  - TSV power 10X < 1nH bonding wire.
  - TSV power 30% < Flip-chip

C. Signal Integrity

- Two well known metrics: Spurious Free Dynamic Range (SFDR) and signal to noise and distortion ratio (SNDR).
  - Transient noise is taken into consideration during simulations.
  - The large inductance and the lower tracking bandwidth degrade the obtained SNDR when bonding wire interface is used.
- SNDR varies by 4 dB for different values of the bonding wire inductance.
- Flip chip shows a 2.5dB degradation in the SNDR.
- TSV results similar to the no-interface case
- SNDR for the 5um and 2um TSVs is within0.1dB.