USC University of Southern California

USC Viterbi School of Engineering

Ming Hsieh Department of Electrical Engineering

# Design Optimization of Deeply-Scaled FinFET-based SRAM Cells under Process Variations

Alireza Shafaei, Shuang Chen, Yanzhi Wang, and Massoud Pedram

## Cache Memories

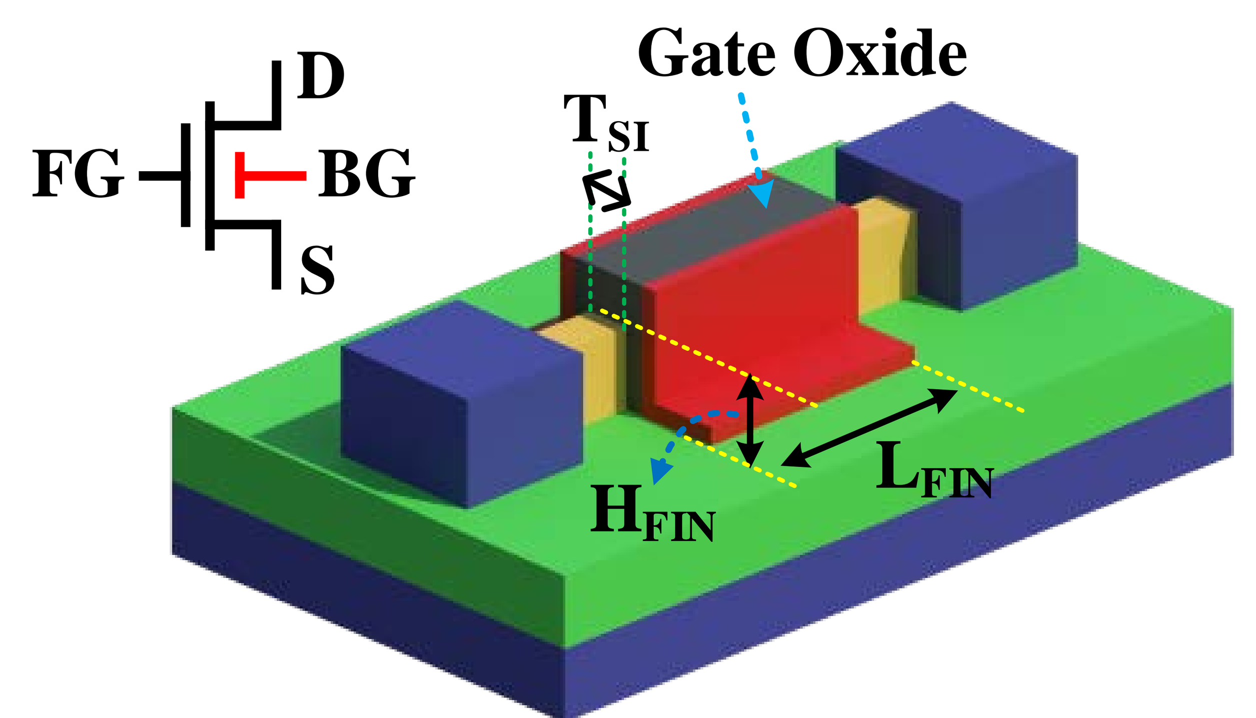
- Occupy a large portion of the chip area
- Have low activity factors (long idle times)

→ High leakage power

- Use minimum size transistors to improve memory density
- Devices with gate length of 7nm and reduced $V_{dd}$

→ Very Sensitive to process variations

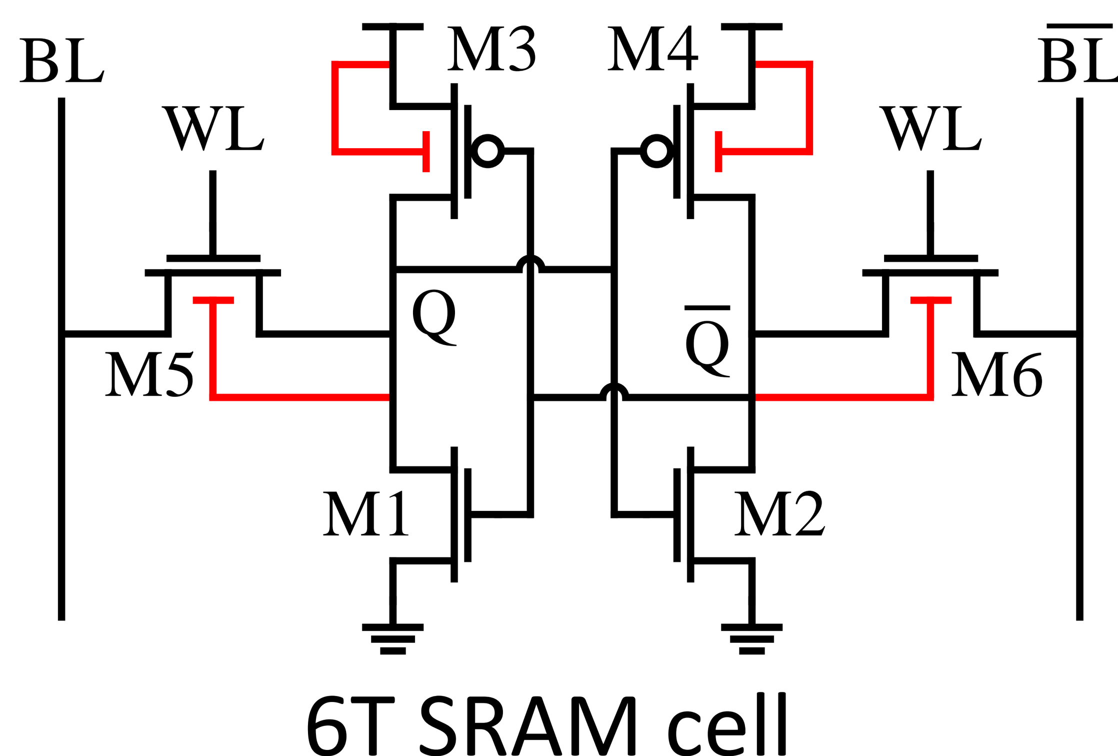
## FinFET Devices



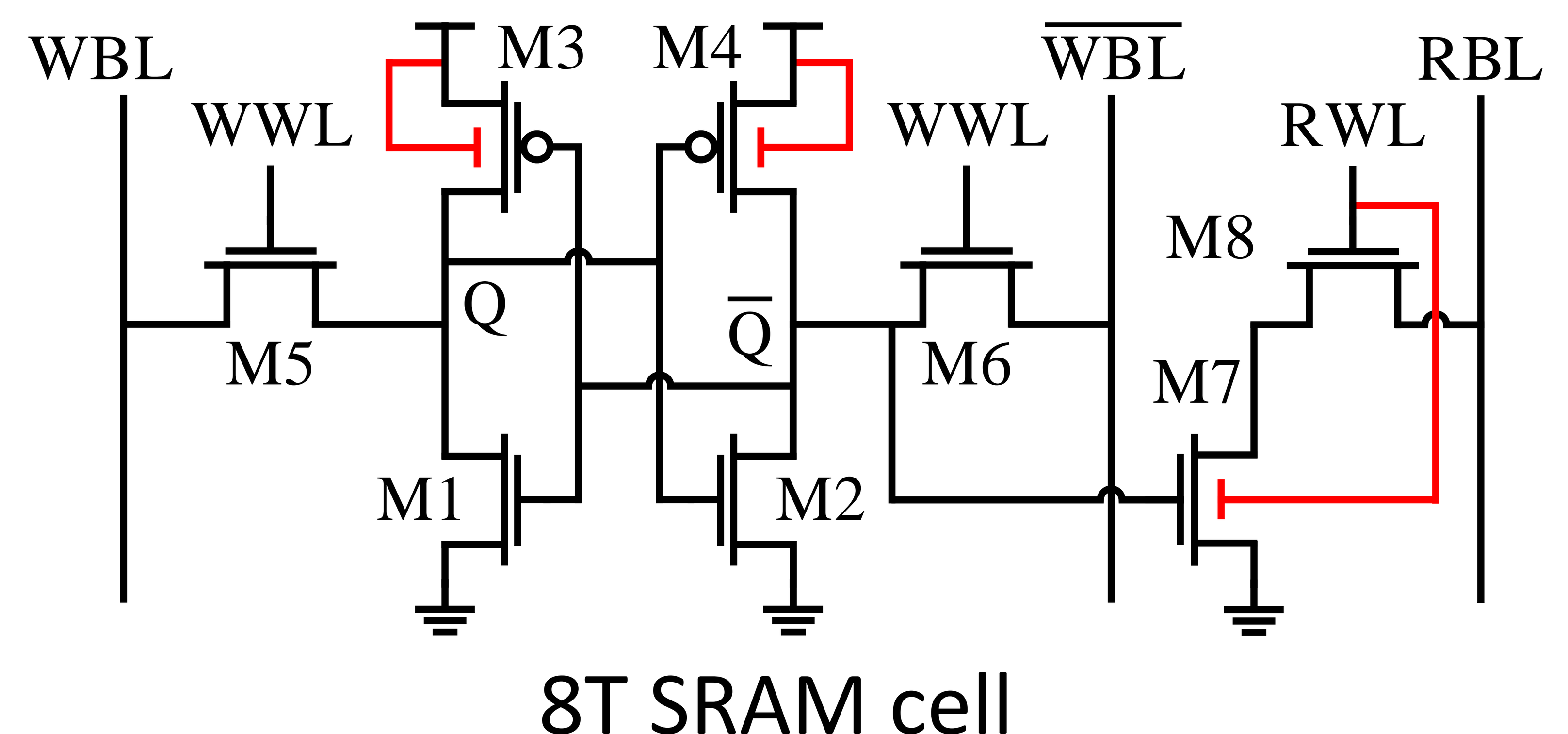

3-dimensional gate control over the channel reduces short channel effects.

## Robust SRAM Cell Design

We use **dual-gate control** of FinFET devices to enhance the SRAM stability.

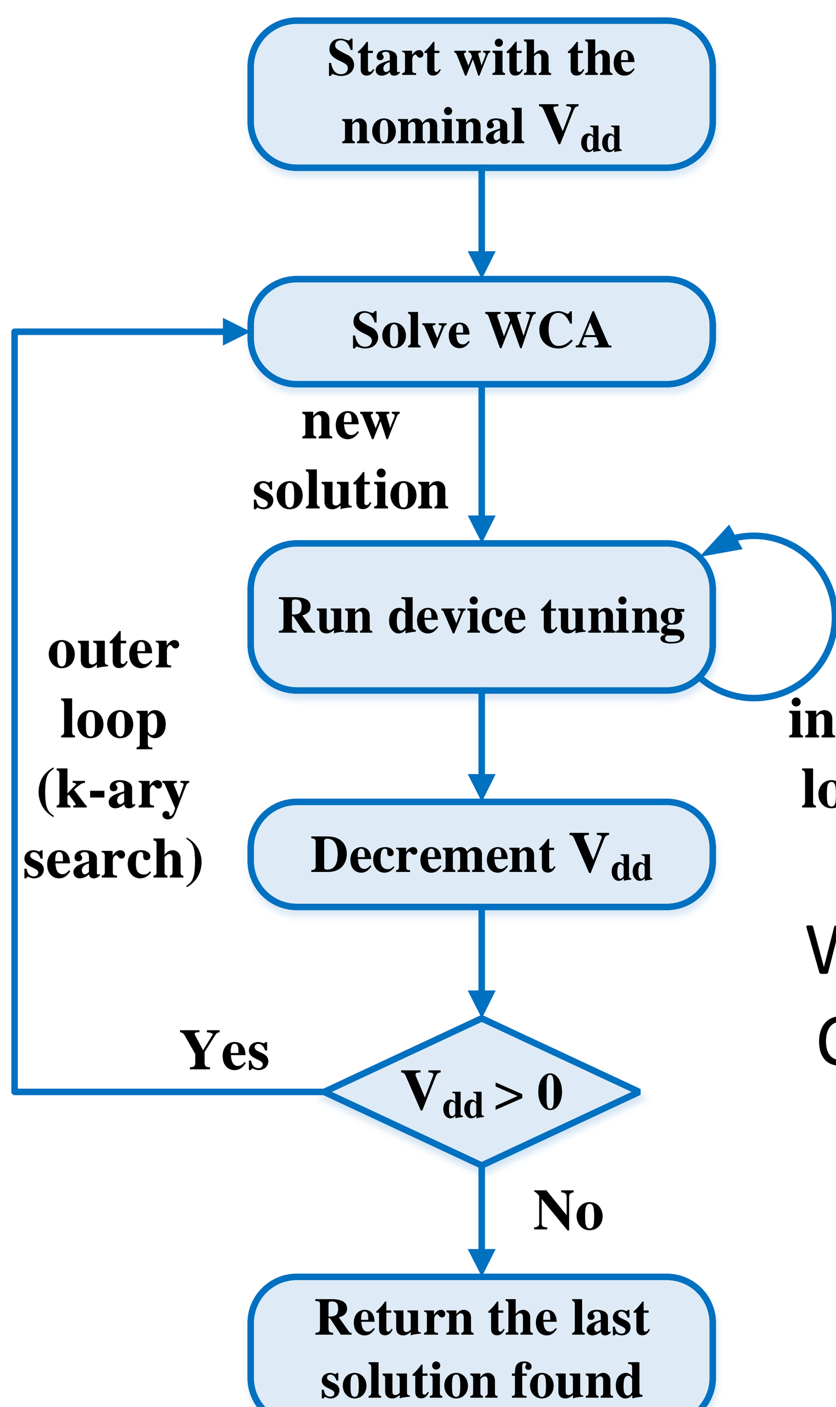



6T SRAM cell




8T SRAM cell

## Design Framework & Results




WCA: Worst-Case Corner of process variation

**Problem statement:** find $V_{dd}$ and transistor-level parameter (number of fins, gate length) values of the SRAM cell in order to minimize the expected leakage energy consumption while yield constraints are satisfied.

**Simulation results for a 4MB, 8-way, L3 cache**

| SRAM Cell | $V_{dd}$ (mV) | Access Latency (ns) | Access Energy (nJ) | Leakage Power (mW) | Area (mm²) |
|---|---|---|---|---|---|
| 6T | 450 | **0.557** | 0.073 | 743 | **0.703** |
| 6T | 324 | 0.793 | **0.041** | **389** | **0.703** |
| 8T | 450 | 0.691 | 0.093 | 802 | 0.980 |
| 8T | 324 | 0.959 | 0.052 | 420 | 0.980 |

**Sponsors:** DARPA PERFECT program and the Software and Hardware Foundations of the NSF.

shafaeib@usc.edu
http://sportlab.usc.edu/~shafaei/

Ming Hsieh Institute
Ming Hsieh Department of Electrical Engineering