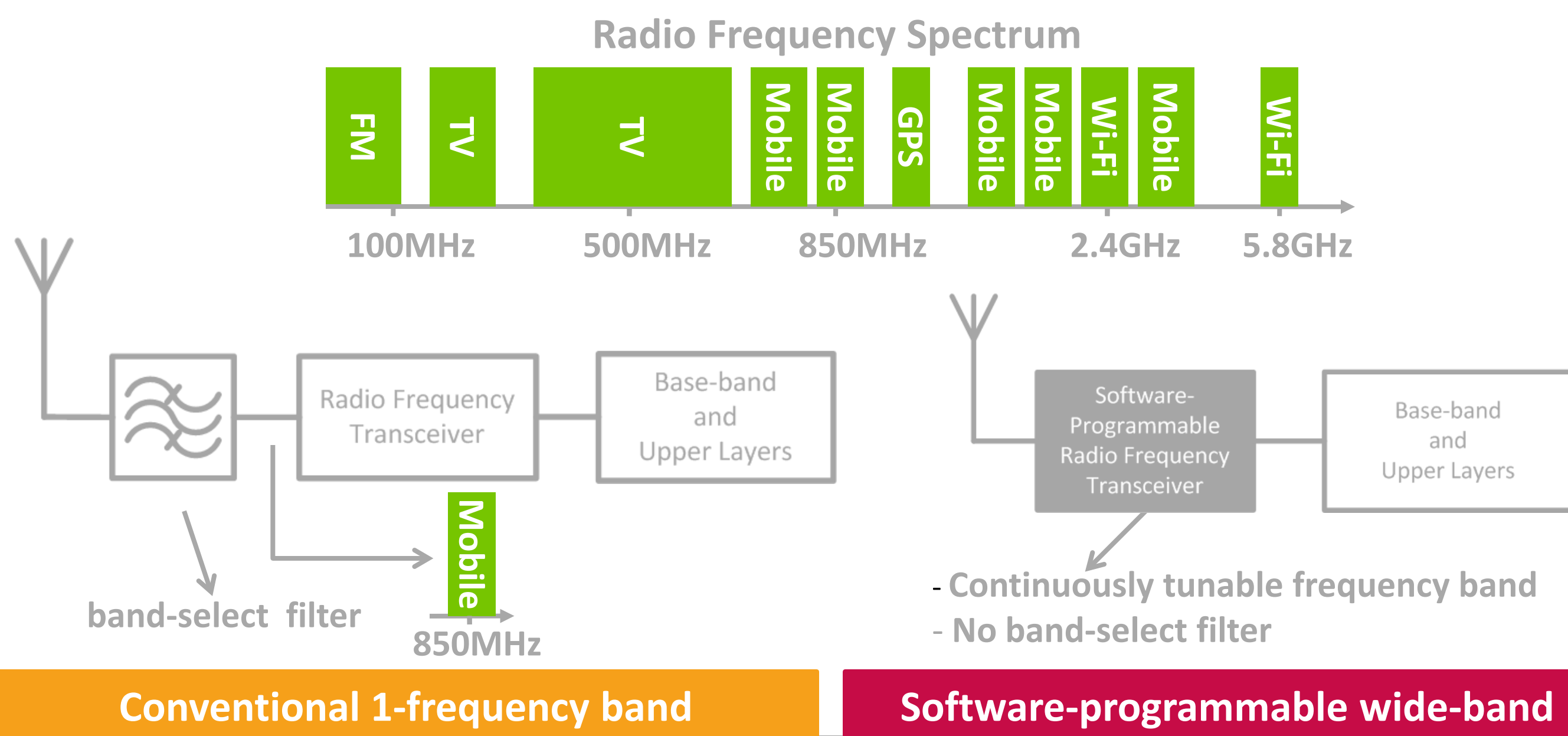


Motivation & Concept



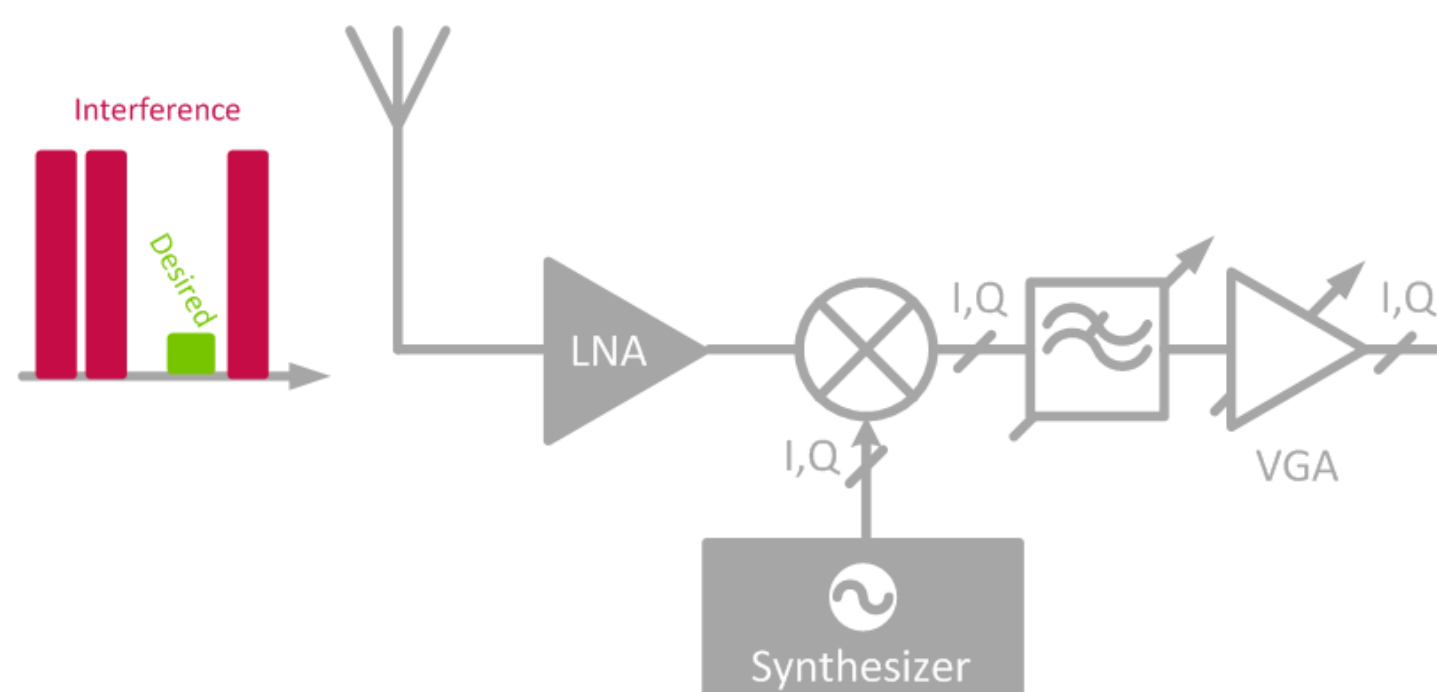
Communication; **anywhere** in the frequency spectrum with **any** modulation

- Cognitive radio
- TV white-spaces
- Multi-band cellular
- RF spectrum sensing
- Counter IED electronic warfare
- **Dynamic spectrum access**

Applications

Key Challenges

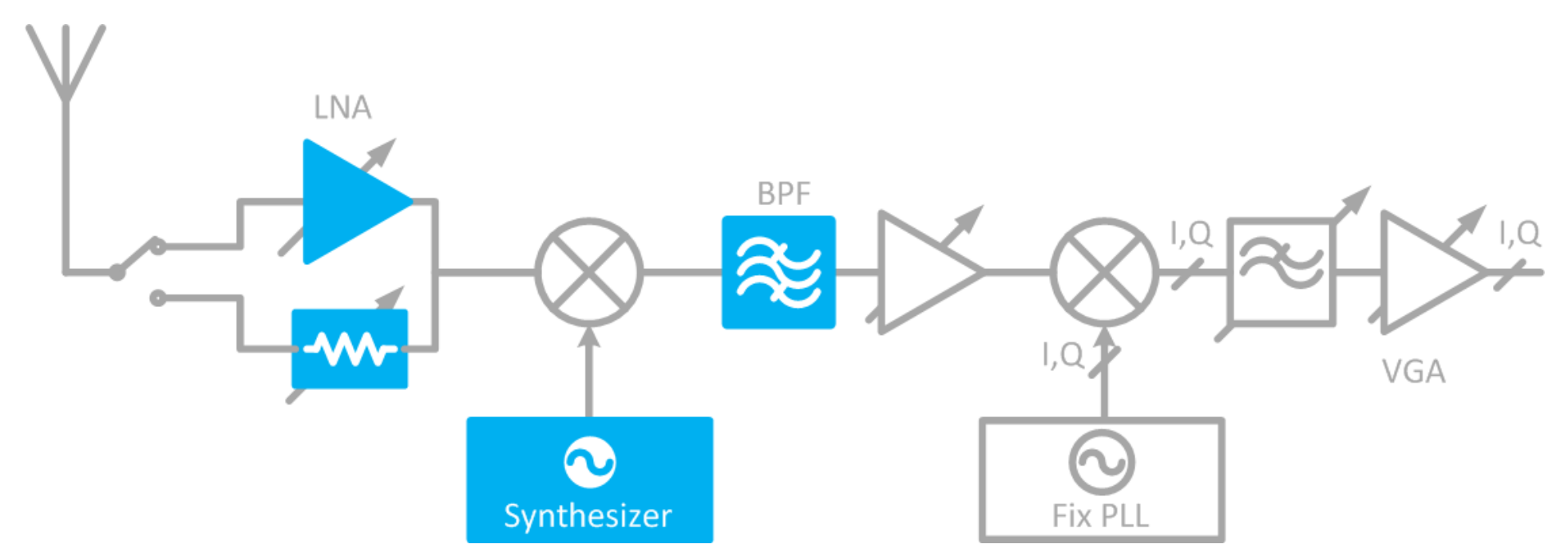
Conventional direct down-conversion architecture



- Large, wide-band **interference**
- Local oscillator (LO) **harmonics**
- **Multi-decade** frequency synthesizer

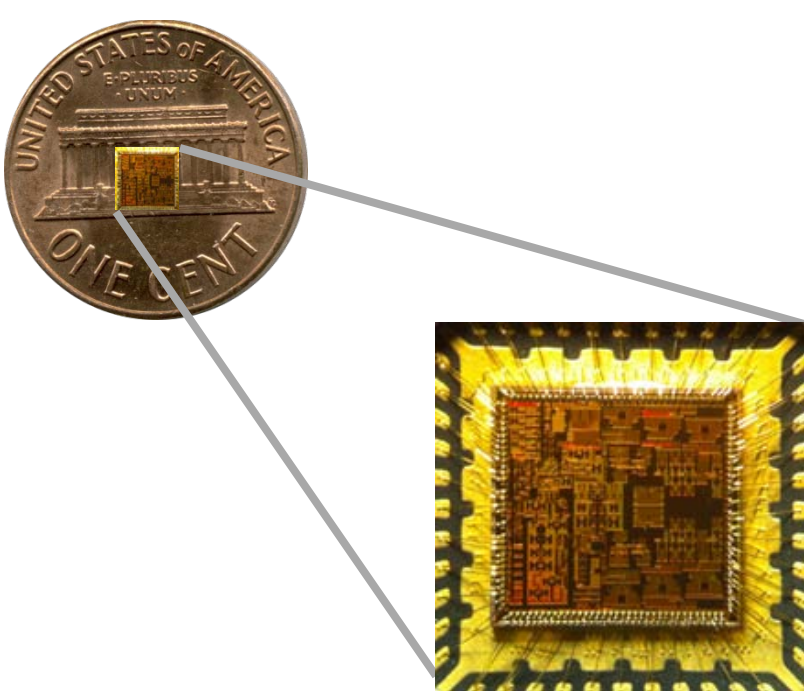
Proposed SDR Solution

Up-down conversion architecture



- LO **harmonic insensitive**
- Fix **on-chip** bandpass filter
- **Low-noise** frequency synthesizer
- **High-dynamic range** front-end

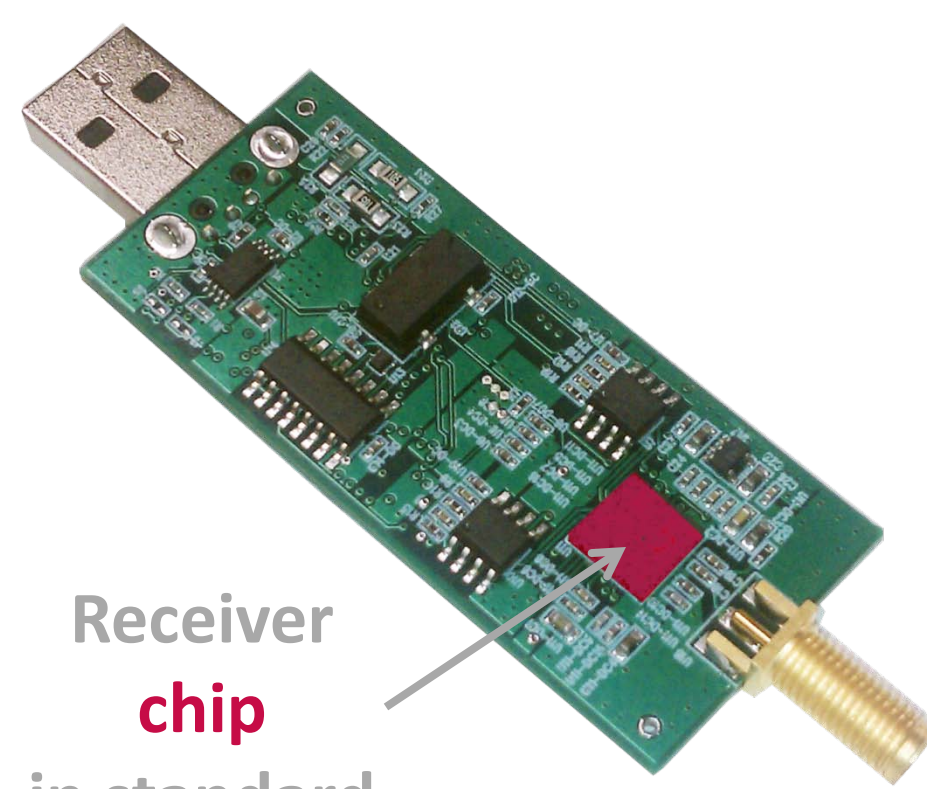
Implementation & Measurement



- **DC-6GHz** receiver
- **0.13μm CMOS**
- **3.7mm x 3.9mm** die size

Silicon chip

USB 2.0 interface



Receiver chip in standard 44-pin QFN

USB evaluation hardware

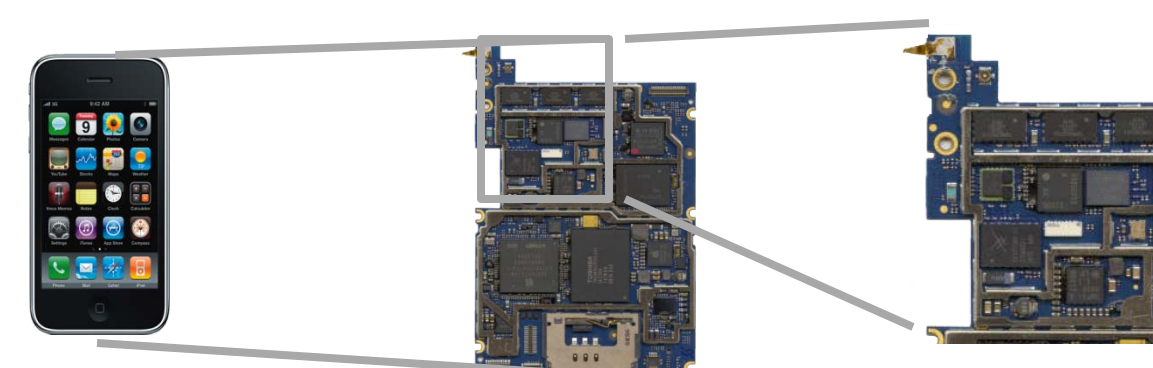
Future Work & Commercialization

Research work in progress

- MIMO software-defined transceiver
- Programmable power amplifier

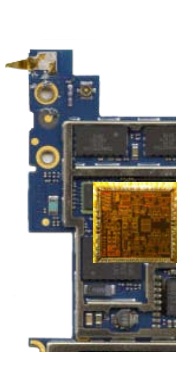
Cellular communication

iPhone's cellular radio transceiver Supports 2G & 3G



Proposed

Proposed chip

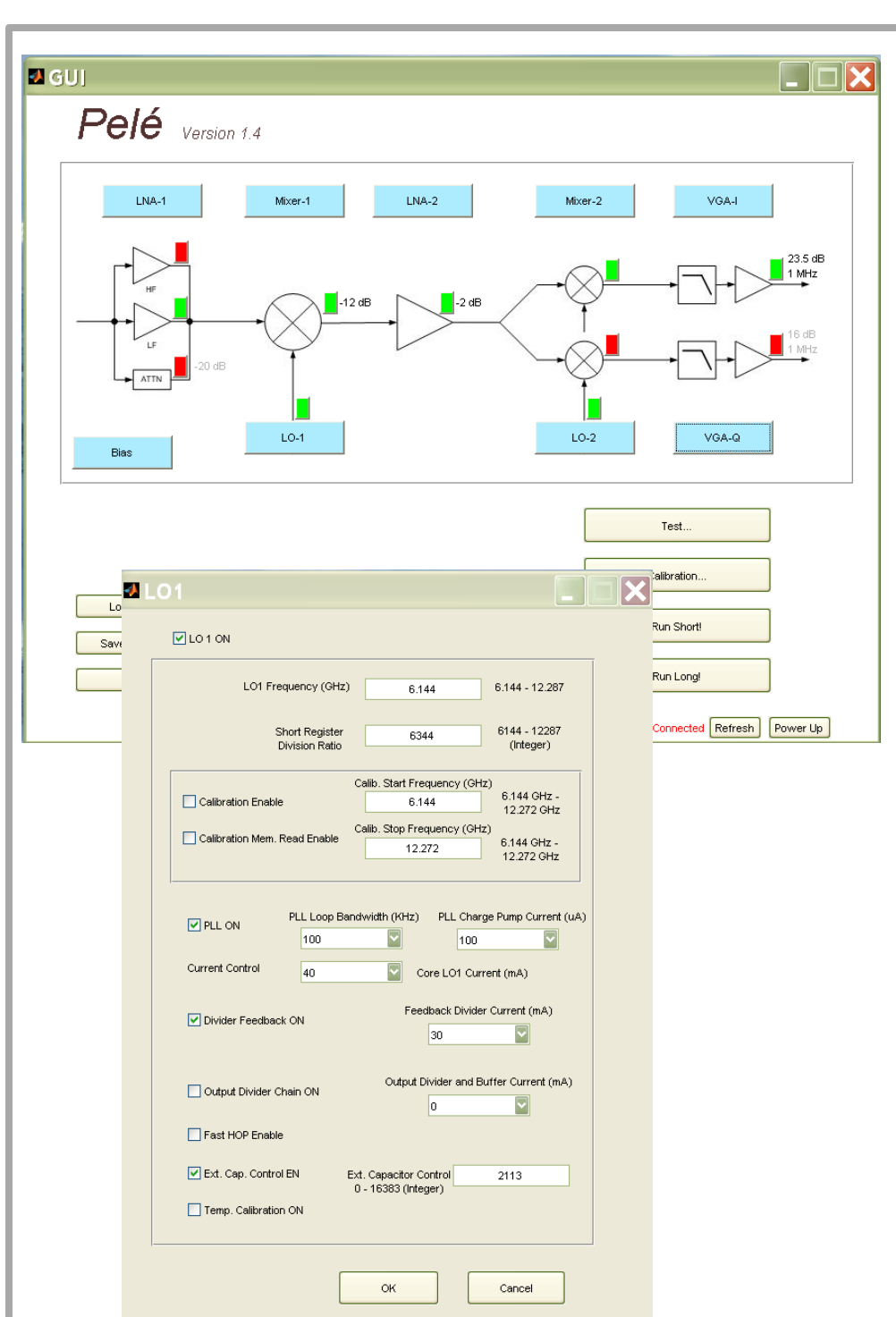


If the proposed transceiver chip is used:

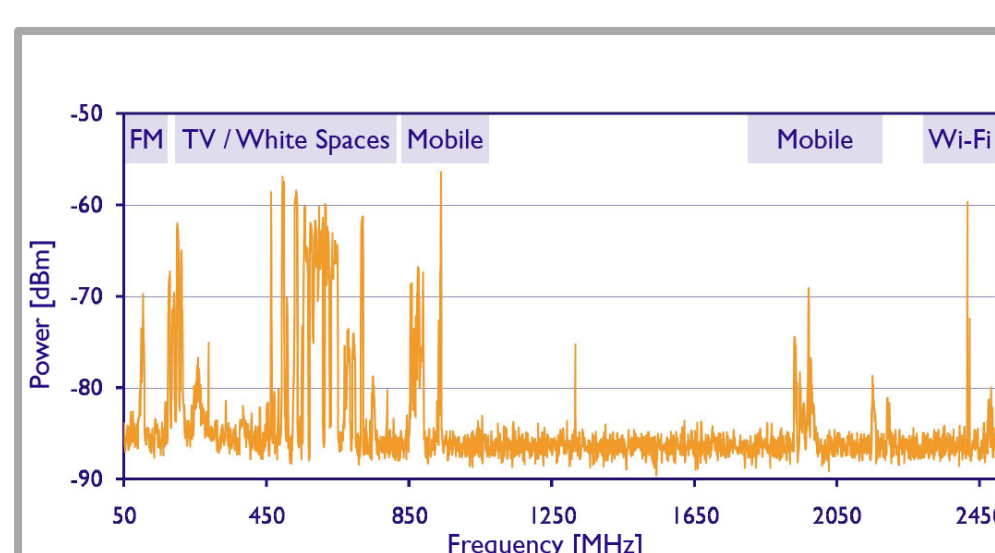
- Supports **all existing & emerging** global frequency bands
- Significant **cost** and **foot-print** reduction
- USPTO patent application 12/727,194 and multiple disclosures

Other applications

- Dismounted RF spectrum sensing for electronic warfare
- Miniaturized instrumentation
- Software-defined tactical radios for defense and public safety



Programming software



Radio frequency spectrum captured by the 1st generation receiver using an external 0.05-2.5GHz antenna. Receiver channel bandwidth is set to 1MHz.

Current measured and next generation expected performance of the Transceiver

	1st Gen RX	Next Gen RX/TX
Frequency Range	DC-6GHz	
Channel Bandwidth	1-22MHz	1-40MHz
RX Sensitivity (1 MHz)	-85dBm	-108dBm
RX SFDR (Co-channel)	43dB	70dB
TX Output Power	N/A	10dBm
Phase Noise (1MHz Offset)	-120dBc/Hz	
Chip Power Consumption	RX: 650mW	RX: 250mW TX: 400mW
Technology	130nm Standard CMOS	

Measurement

Recognitions

- **Best student paper** award candidate, IEEE RFIC 2011
- A. Goel, B. Analui, H. Hashemi, "A 130nm CMOS 100Hz-6GHz Reconfigurable Vector Signal Analyzer and Software-Defined Receiver," IEEE RFIC Symposium, June 2011.
- **Inaugural winner:** USC Maseeh Entrepreneurship Prize Competition
- Sponsors: ONR JCREW EW S&T and DARPA
- Other acknowledgements:

