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Method of Measuring Accurate Dynamic Power Consumption of Integrated Components and Sub-circuits

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INTRODUCTION

Background

The most common run-time power measurement method for integrated circuits require analog probes, current sense resistors, and dedicated ADCs. This measurement method tends to be costly and often presents calibration, performance, power, and scalability constraints; especially when it is applied to a system where a large number of components need to be monitored. We present an alternative solution that uses digital measurements and applied mathematics to achieve greater accuracy and temporal resolution at finer subcomponent granularity, greatly reduced cost and smaller physical size.

Source : www.skytower.md

Goals

- Identify the nature of power dissipated and commonly used applied mathematical techniques.
- Develop method that can be commonly applied to various systems.
- Build a prototype system to test with actual hardware and compare the results of the proposed method and actual power measurement.

Advantages

Less Invasive

- The weights are calculated using total system power measured via ADC.
- Minimal instrumentation of digital monitoring devices effectively reduces introduction of noise in the measurements.

Less Power

- A instrumentation of digital counters in the ASIC

Lower Cost

- All digital components (no mixed signal processing)
- No need for calibration and replacement of devices.

Increased Performance and Scalability

- Measurement resolution at the lowest level
- The same level of accuracy for any number of components.

SIGNAL ACTIVITY BASED COMPONENT ANALYSIS

Motivation

- Low power and minimally invasive power monitoring method allows efficient and intelligent power management.

Approach

- Add digital counters to all relevant pins and wires to capture their signal activities.
- Apply independent component analysis to the counter values and the total measured power to obtain weights for the signal transition for each component.
- Use the power weights previously calculated measure actual power.

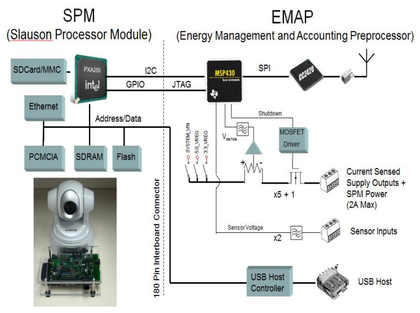
RELATED WORK

Energy Aware Processing

- Direct sub-component power measurement via current sense resistors and dedicated ADCs.
- Use fine grained power monitoring to dynamically schedule instructions (LEAP/LEAP2).

Drawbacks

- Not scalable.
- High speed and accurate ADCs cost are costly
- ADC aging, calibration and subsequent replacements are difficult and expensive.



LEAP Architecture : McIntire, et al.

FUTURE WORK

- Precisely evaluate the technique with a revised reconfigurable system (NetFPGA) with the traditional power monitoring instruments that allows capturing of the ground truth.
- Show that the idea scales up to much more complex designs like a modern PC or large router.

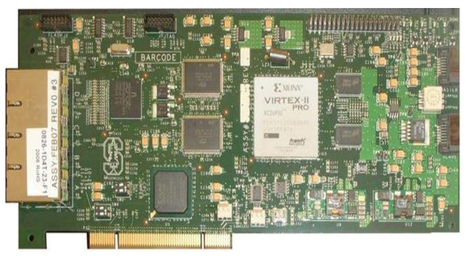
PROTOTYPE SYSTEM

Proof-of-Concept System

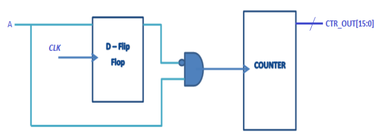
- Reconfigurable hardware/software co-design network appliance (NetFPGA).
- DAQ to monitor the total power
- Time synchronization between digital and analog measurements
- ICA based power weight derivation

Baseline Measurements

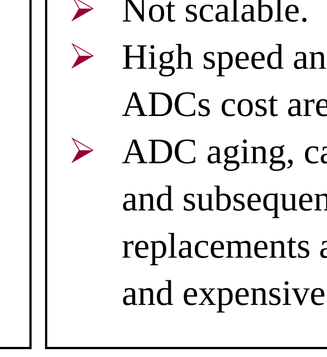
- IP router (NetFPGA) connected to 4 PCs exchanging packets at 1Gbps.
- Training data was captured for deriving power weights
- Additional data can be used to estimate and evaluate the power measurement method



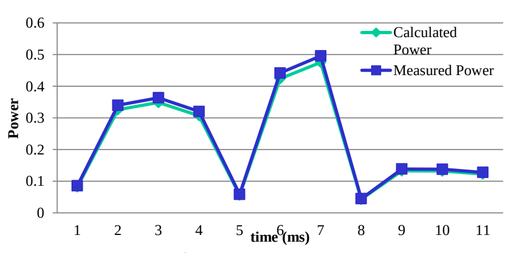
NetFPGA Board



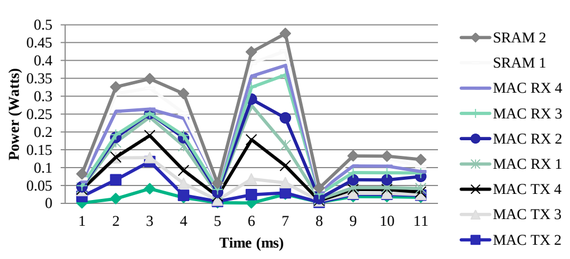
Counter module for each pin monitored



Reference pipeline design - NetFPGA



Comparison of measured and calculate TOTAL dynamic power over time



Dynamic Power Per-component

EXPERIMENT SETUP

Objectives

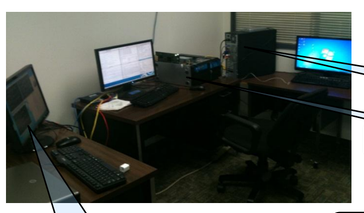
- Operate instrumented system at different scenarios
- Collect, derive, and compare power data to the ground truth measurements

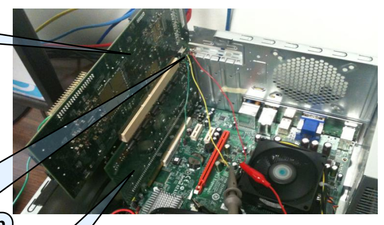
Approach

- Fully connect the system and exercise it at various scenarios including intermediate loads.
- Collect total power and the counter values.
- Regression testing and evaluation.

Conclusion

- Currently, component level measurement is not feasible using traditional method due to limited instrumentation.
- Limited experiments show that there is a maximum of 7% difference between the traditional ADC method and our digital method in terms of total power





Packet generators

NetFPGA 1G Board

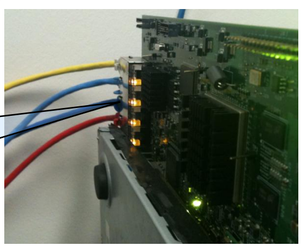
Host : Tracer DAQ

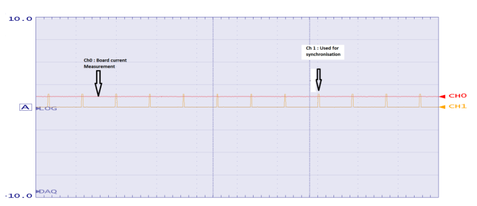
Host :NetFPGA

Current sampling points on power measurement board. (5V,3.3V and GND)

PCI extender

All 4 ports connected to exercise maximum network load





Current measurement through DAQ

Patent Details : Patent Pending
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