Ming Hsieh Department of Electrical Engineering

Software-Defined Radio (SDR) Receiver Using Sample Domain Signal Processing (SDSP)

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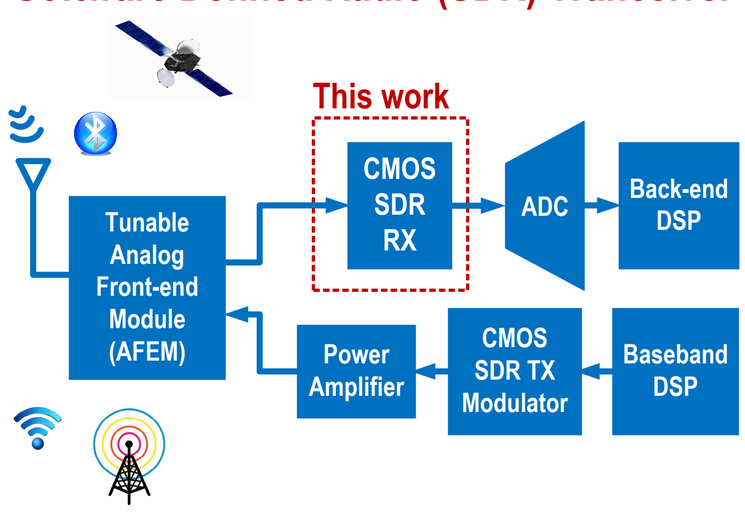
Research Objective

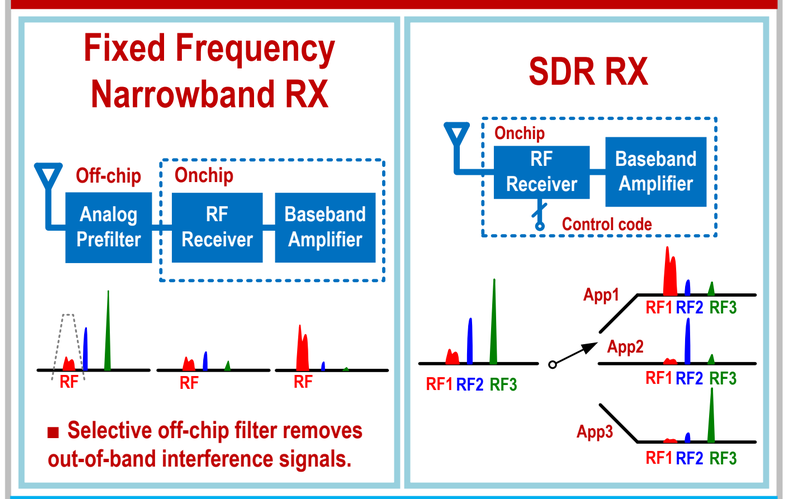
Software Defined Radio (SDR) Tranceiver



- Wide radio frequency range
- Various wireless communication modulations

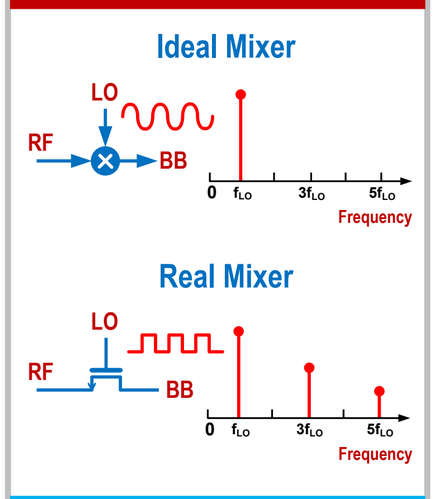
SDR RX Main Challenges

Dynamic Range



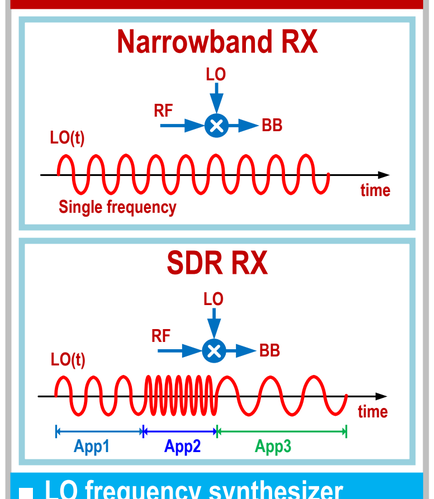
- Selective compact tunable prefilter is still not available, therefore, the SDR RX should have a high dynamic range.

Harmonic Rejection



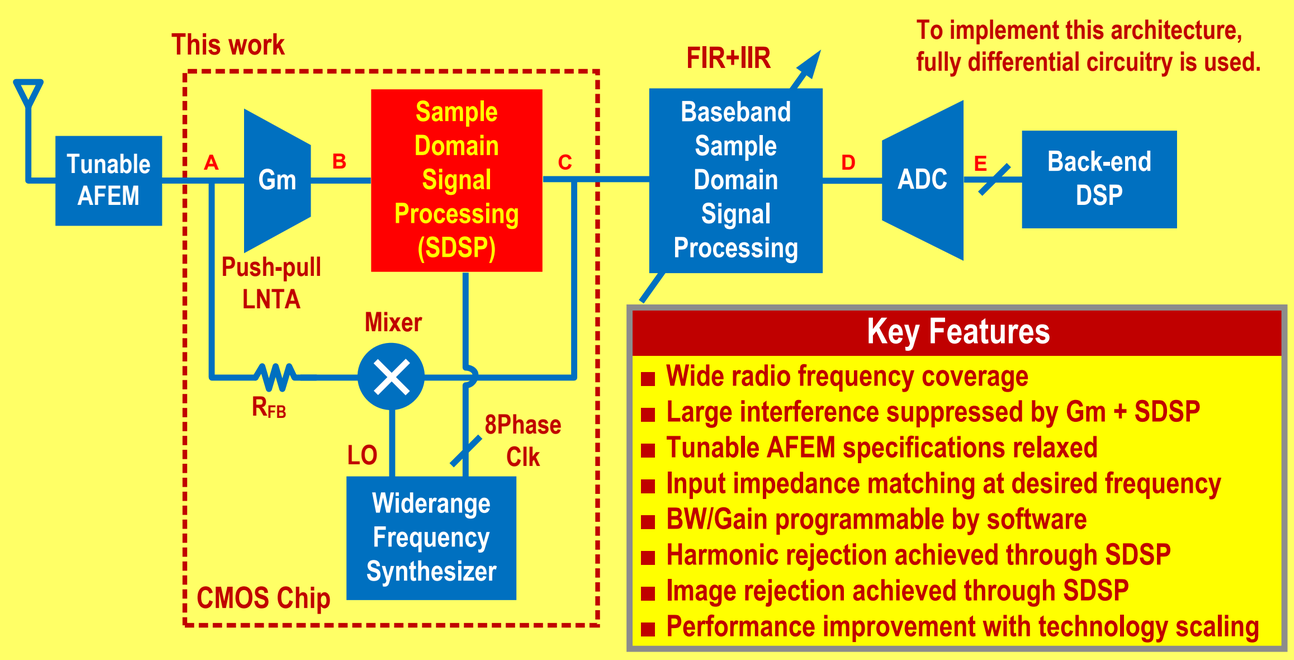
- Signals at LO harmonics fold on top of the desired signal.

LO Synthesizing



- LO frequency synthesizer should cover wide frequency range with low phase noise.

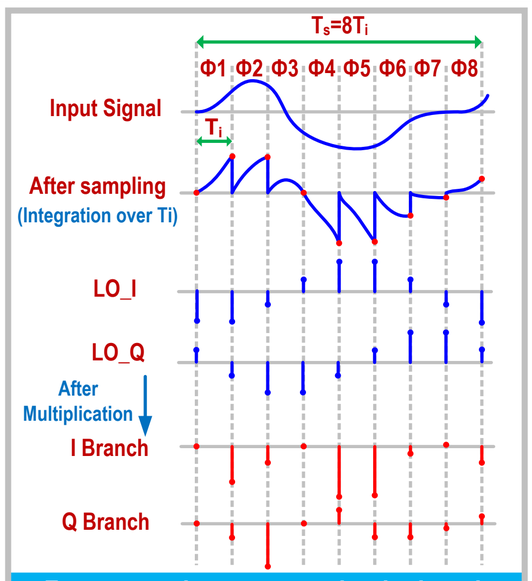
Proposed Architecture



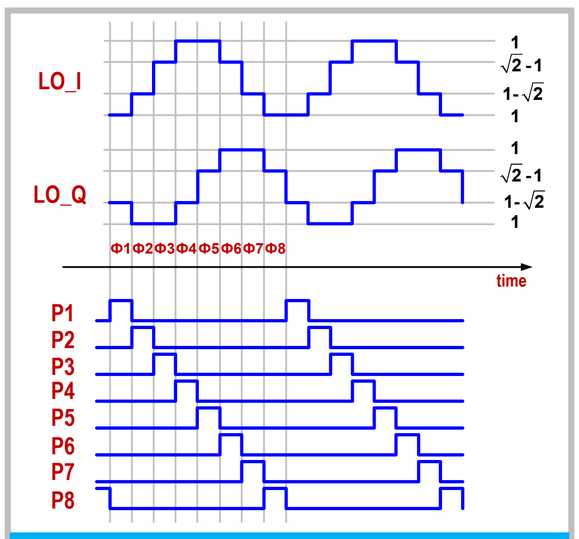
Key Features

- Wide radio frequency coverage
- Large interference suppressed by Gm + SDSP
- Tunable AFEM specifications relaxed
- Input impedance matching at desired frequency
- BW/Gain programmable by software
- Harmonic rejection achieved through SDSP
- Image rejection achieved through SDSP
- Performance improvement with technology scaling

SDSP Concept



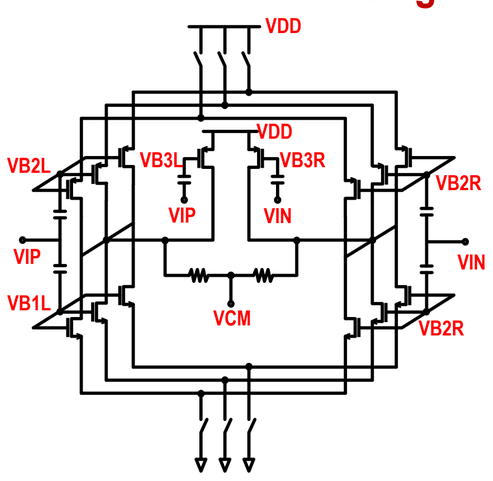
- Frequency down conversion is done in charge domain



- 8-phase non-overlapping clock (P1 - P8) is required in order to achieve both image rejection and harmonic rejection.

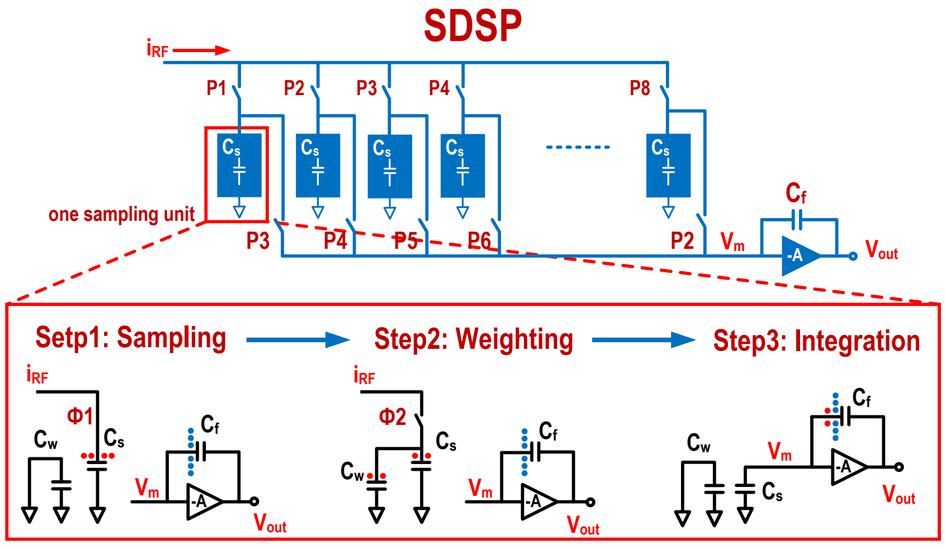
Integrated Circuit Implementation

RF Front-end Gm Stage



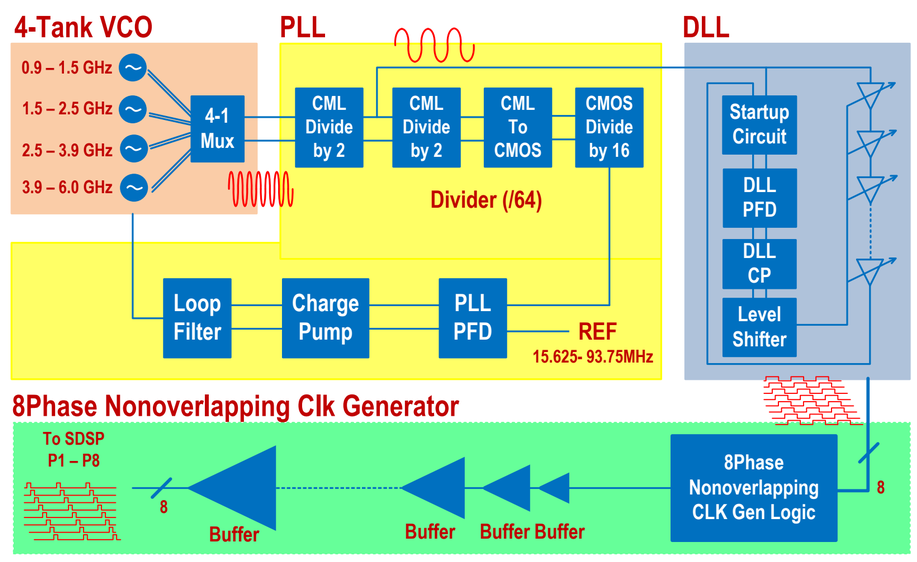
- Inverter-based Gm stage
- Large input swing handling
- Gain programmable

SDSP



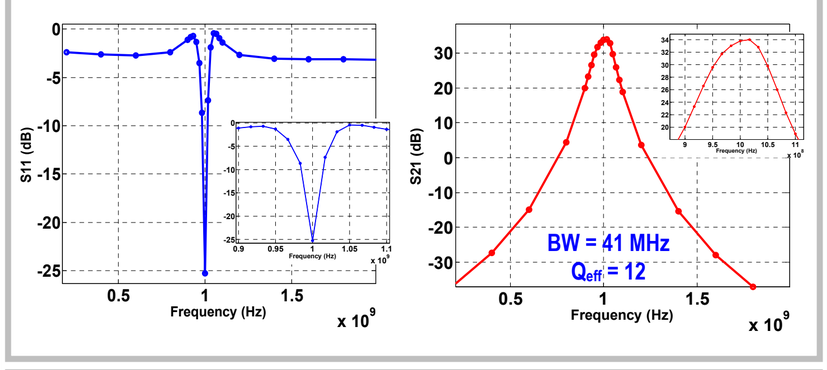
- The implemented circuit is fully differential and contains I and Q branches.
- Transfer function contains two poles: 40 dB/dec filtering

SDSP Clock Generator

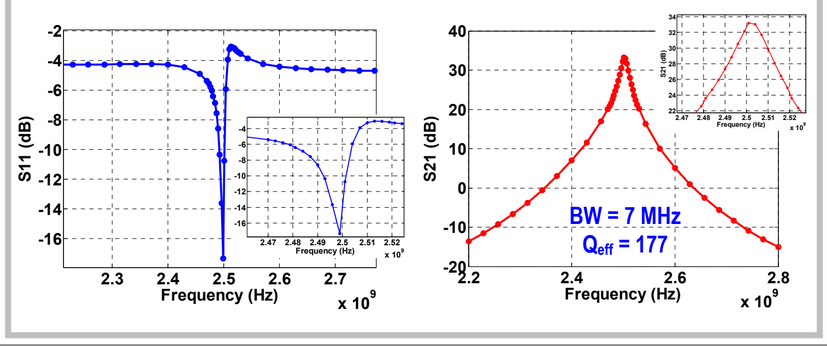


Simulation Result Highlight

Simulated S Parameters @ f_s = 1 GHz



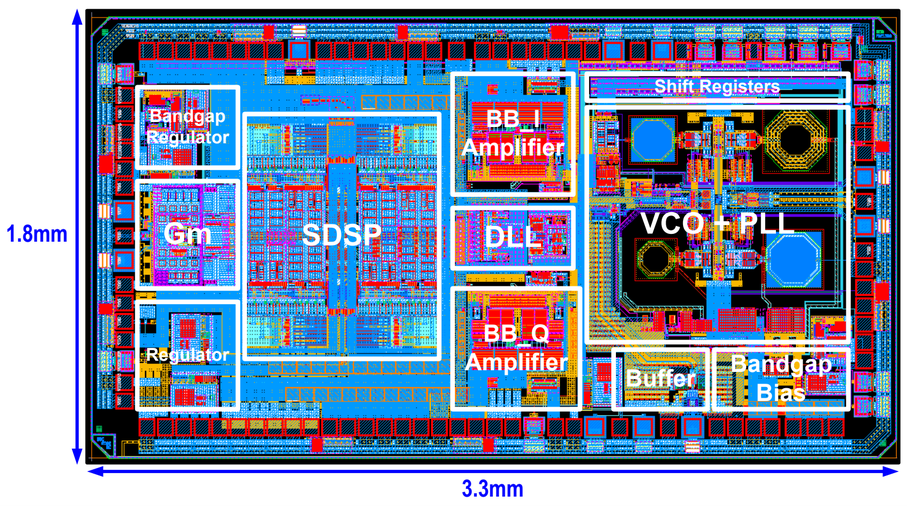
Simulated S Parameters @ f_s = 2.5 GHz



Design Summary

	Achieved By Simulation
Technology	65nm LP CMOS
Frequency range	0.5 GHz ~ 3 GHz
Tuning resolution	Continuous
S_{11}	< -15 dB
S_{21}	34 dB
NF	6.5 dB
IIP3 (OB)	3 dBm
ICP_{1dB}	-29 dBm
OCP_{1dB}	2.7 dBm
HR3	> 56 dB
RF chain power consumption	146 mW
Clock power consumption	106 mW ~ 440 mW
Total power consumption	252 mW ~ 586 mW
V_{dd}	1.2 V (Core) 2.5 V (Bandgap + Reg.)

Chip Layout



Conclusion

- Proposed a solution for SDR RX based on SDSP
- Support various wireless communication bands from 0.5~3 GHz
- Decent frequency selectivity and high dynamic range, robust to interference
- Decent harmonic rejection and image rejection
- Gain/BW fully programmable
- Good for technology scaling down

Future Work

- High dynamic range SDR TX design based on SDSP
- Integrate the entire SDR transceiver
- Study the fundamental limit of SDSP system power consumption
- Design the reconfigurable front-end module for SDR transceiver

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