Software-Defined Radio (SDR) Receiver Using Sample Domain Signal Processing (SDSP)

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Research Objective
Software Defined Radio (SDR) Transceiver

- Tunable Analog Front-end Module (AFEM)
- CMOS Low-Power ADC
- CMOS SDR RX Modulator
- Power Amplifier
- Back-end DSP

Proposed Architecture

- Sample Domain Signal Processing (SDSP)
- Wideband Frequency Synthesizer
- Key Features:
  - Wide radio frequency coverage
  - Large interference suppression by Gm + SDSP
  - Tunable AFEM specifications relaxed
  - Input impedance matching at desired frequency
  - BV/LV gain programmable by software
  - Harmonic rejection achieved through SDSP
  - Image rejection achieved through SDSP
  - Performance improvement with technology scaling

Integrated Circuit Implementation

- RF Front-end Gm Stage
- SDSP
- Design Summary:
  - Achieved by Simulation:
    - Technology: 65nm LP CMOS
    - Frequency range: 6.5 GHz – 3 GHz
    - Tuning resolution: Continuous
    - Input SW: 100
    - NF: 6.5 dB
    - IIP3 (dBm): 5 dBm
    - CMRR: -20 dB
    - CHRR: 2.7 dBm
    - VDD: 1.5 V
    - RF chain power consumption: 146 mW
    - Clock power consumption: 106 mW – 440 mW
    - Total power consumption: 252 mW – 166 mW
    - VCM

Simulation Result Highlight

- Bandwidth
- Linearity
- Harmonic rejection
- Power consumption

SDSP Concept

- S-phase Non-overlapping clock (P1 - P8) is required to achieve both image rejection and harmonic rejection

SDSP Clock Generator

- PLL
- Charge Pump
- Voltage Controlled Oscillator (VCO)
- Divider (N)

Chip Layout

- High-dynamic range SDR TX design based on SDSP
- Design the reconfigurable front-end module for SDR transceiver

Conclusion

- Proposed a solution for SDR RX based on SDSP
- Support various wireless communication bands from 0.5-3 GHz
- Decent frequency selectivity and high dynamic range, robust to interference
- Decent harmonic rejection and image rejection
- Gain/BW fully programmable
- Good for technology scaling down

Future Work

- Study the fundamental limits of SDR system power consumption
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- Design the reconfigurable front-end module for SDR transceiver

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