Ming Hsieh Department of Electrical Engineering

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Watt-Level Efficient Linear Power Amplifier in Silicon

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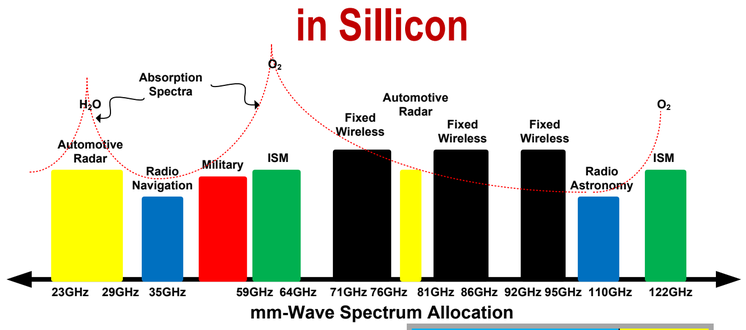
Research Objective

Watt-Level Efficient Linear Power Amplifier in Sillicon



- High Data Rate Wireless Communication
- Active Radars
- Active mm-Wave Imaging

Technology	BiCMOS
Frequency	45 GHz
Peak Power	36 dBm
Power Added Efficiency (PAE) at peak power	65%
RF Bandwidth	3.5 GHz
Data rate (64 QAM)	0.520 Gbps
Bandwidth	100 MHz
Error Vector Magnitude (EVM)	< 2%
ACPR @ 1*BW_{ch}	< −55 dBc

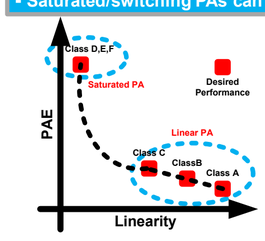
Research Challenges

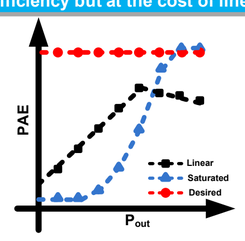
Technological Constraints

- Breakdown voltage of transistors scale down with increasing f_T & f_{max}.
  - $V_{breakdown}$ < 6 V (in 130nm SiGe process), hinders watt-level power generation.
- Efficiency decreases with frequency due to -20 dB/dec roll off in power gain.
- Higher ohmic loss in passives at higher frequency (due to lower skin depth) degrades efficiency.

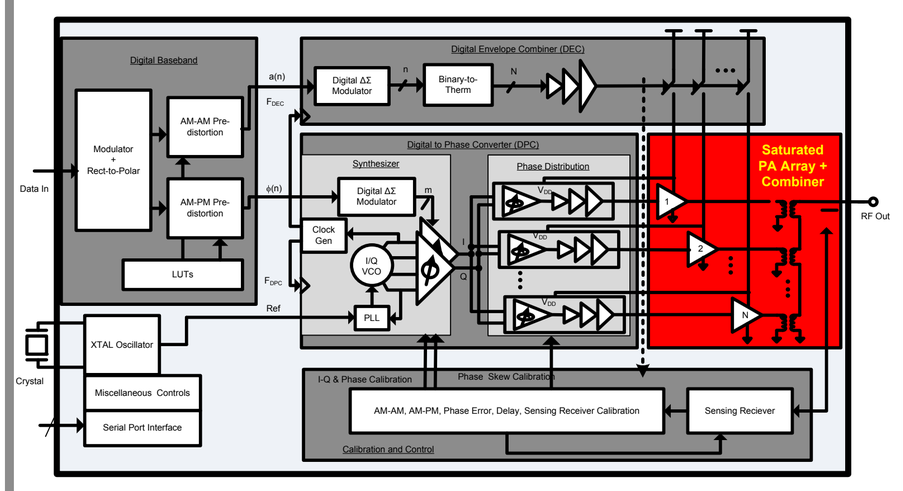
Topological Constraints

- Peak efficiency in linear PAs degrade with power back-off.
- Maintaining high efficiency with power back off is essential for modulating signals with high Peak to Average Power Ratio (PAPR) (as in OFDM).
- Saturated/switching PAs can give higher efficiency but at the cost of linearity.



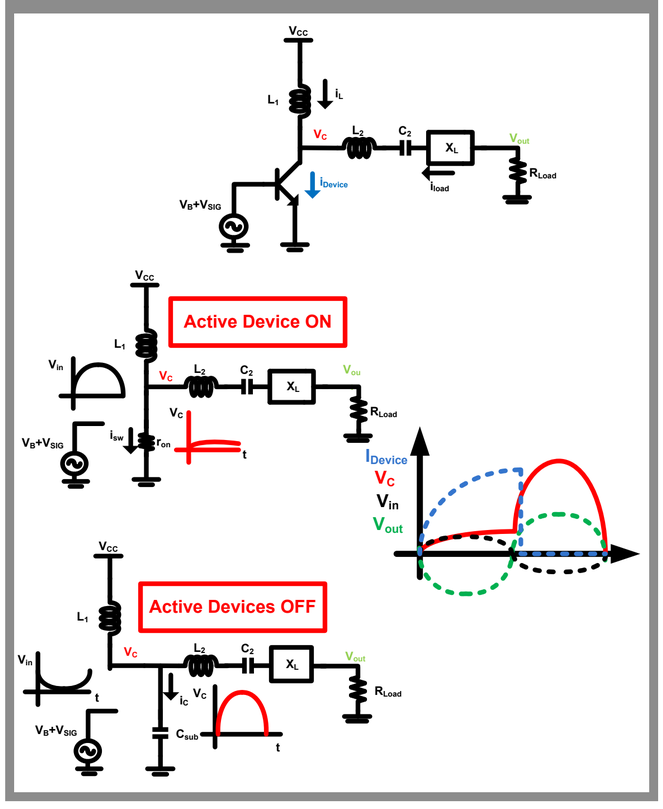


Digital Polar Transmitter (DPT)



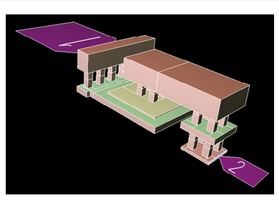
- Saturated/switching class PAs in individual power modules for high efficiency.
- Amplitude modulation using low-loss switching supplies.
- Phase modulation using phase-shifters.
- ΔΣ modulators for minimizing in-band quantization noise.
- Digital polar architecture ensures high PAE at both peak and average power.

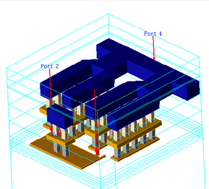
Class-E PA Concept



Implementation Issues

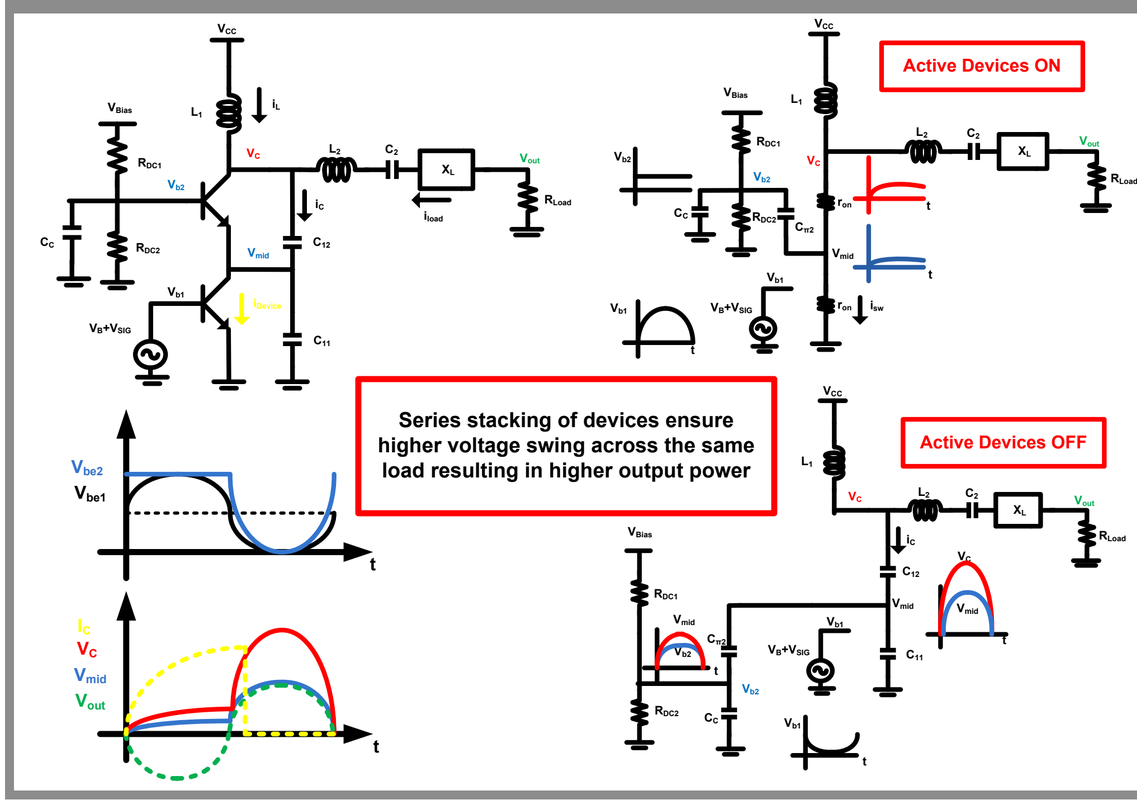
- High V_{CC} (for higher P_{out}) causes avalanche induced base instability.
- Interconnect parasitic degrade f_{MAX} of the device and lower performance.
- Passive networks must be properly chosen to have high enough self resonating frequency.



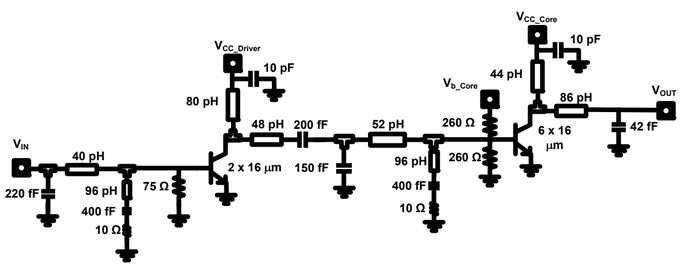


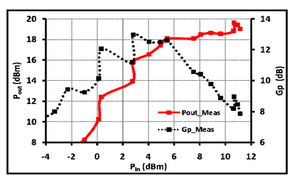
- Passive structures and interconnect are modeled using electromagnetic simulators.
- Small signal and large signal stability are analyzed using periodic steady state simulations.
- Avalanche phenomenon can be alleviated by using series stacking of transistors to increase stability margin without compromising power and PAE performance.

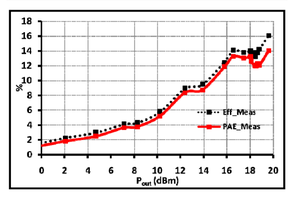
Series Stacking of Class-E PAs

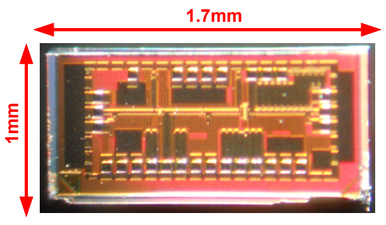


Single Stage Class-E PA



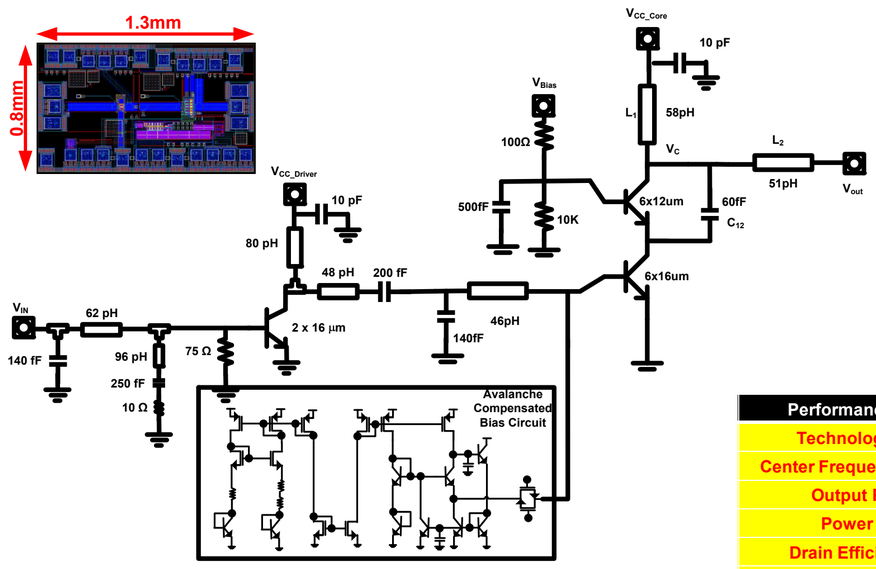


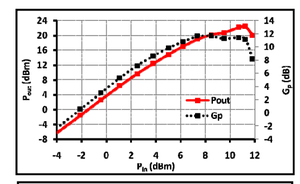


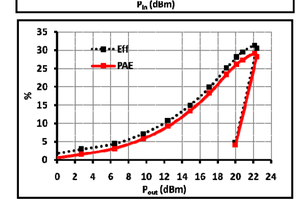


Performance at Peak P_{out}		
Performance Metric	Simulated Performance	Measured Performance
Technology Node	IBM 130nm SiGe BiCMOS	IBM 130nm SiGe BiCMOS
Center Frequency / BW_{-1dB}	39 GHz / 3.5 GHz	39 GHz / 4 GHz
Output Power	19.2 dBm (84 mW)	19.6 dBm (91 mW)
Power Gain	8 dB	8.9 dB
Drain Efficiency (η)	25.5%	16.1%
PAE_{MAX}	21.4%	14%

Double Stacked Class-E PA

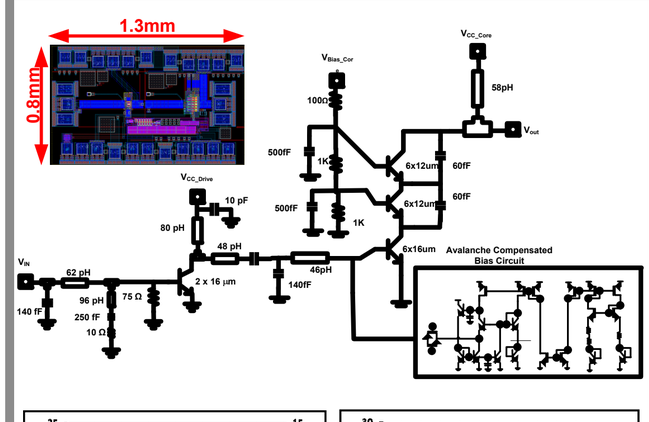


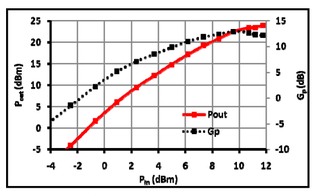


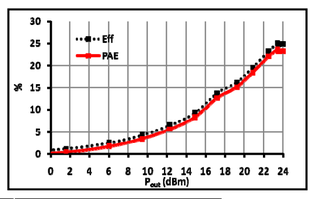


Performance Metric	Simulated Performance
Technology Node	IBM 130nm SiGe BiCMOS
Center Frequency / BW_{-1dB}	45 GHz / 4 GHz
Output Power	22.15 dBm (165 mW)
Power Gain	11.5 dB
Drain Efficiency (η)	31.5%
PAE_{MAX}	29%

Triple Stacked Class-E PA

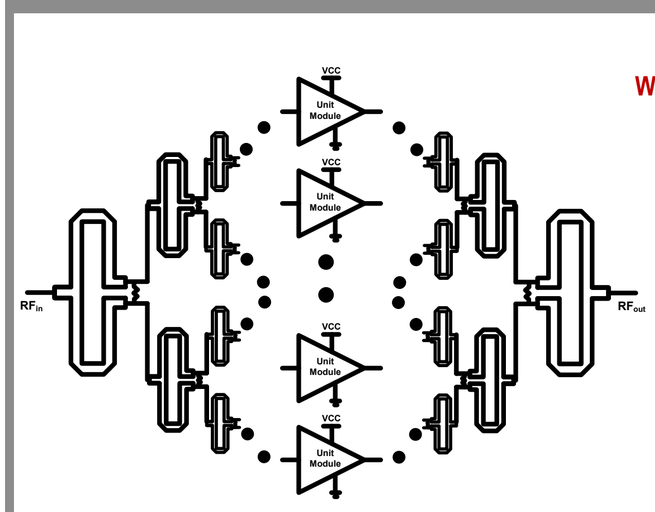


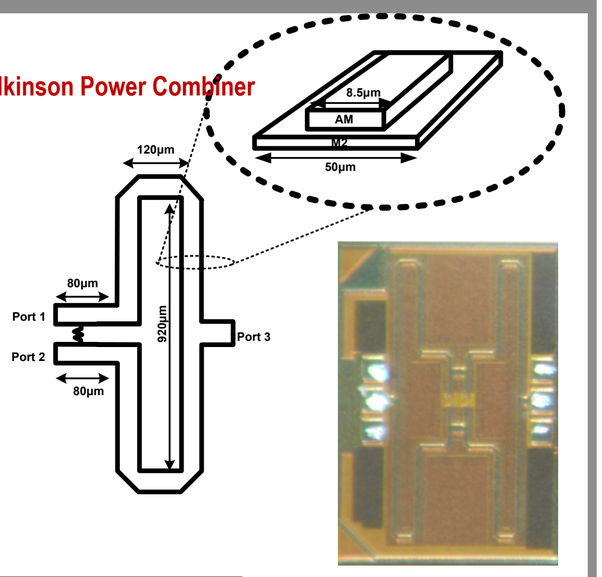




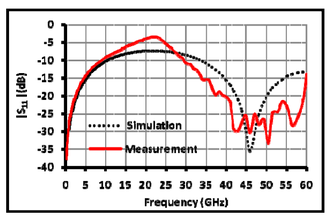
Performance Metric	Simulated Performance
Technology Node	IBM 130nm SiGe BiCMOS
Center Frequency / BW_{-1dB}	45 GHz / 4 GHz
Output Power	23.4dBm (220 mW)
Power Gain	12.7dB
Drain Efficiency (η)	25%
PAE_{MAX}	24%

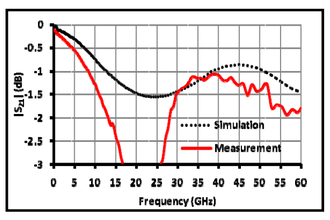
Low Loss mm-Wave Power Combiners





Control Bits (n)	Unit Module Output Power (P_{out})	Total Power Combining Loss (0.5dB per combiner)	Total Output Power (P_{out_Total})	P_{out_Total} Resolution (2^n)	System PAE (25% PAE per unit module)
2	25.0dBm (316mW)	1.0dB	30dBm	4	19.8%
3	22.5dBm (176mW)	1.5dB	30dBm	8	17.6%
4	20.0 dBm (100mW)	2.0dB	30dBm	16	15.6%
5	17.5 dBm (56mW)	2.5dB	30dBm	32	14%





Future Research

- Measurement of stacked devices.
- Large signal characterization and modeling of SiGe HBTs.
- Designing other blocks of the digital polar transmitter.
- Large signal nonlinear stability analysis.
- Deriving efficiency limit of active devices in power amplifier implementation.
- Analyzing trade-off of performance vs stability in mm-wave power amplifiers.

Sponsors

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