Modeling the Impact of TSVs on Average Wire Length in 3DICs using a Tier-Level Hierarchical Approach

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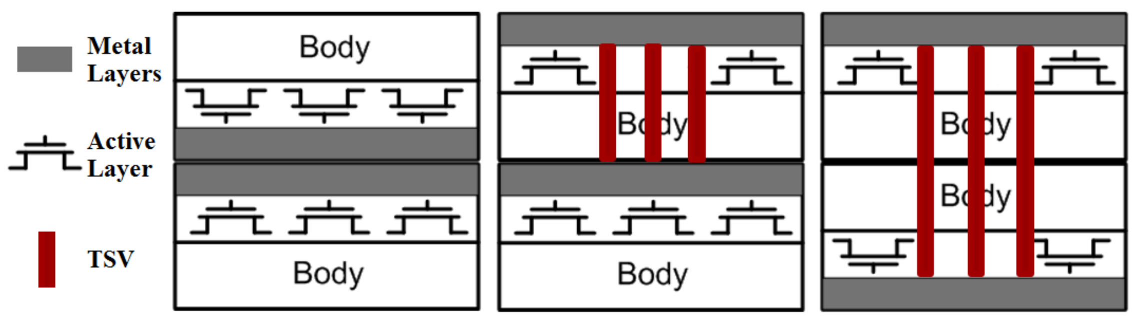
3DIC

- In a three-dimensional integrated circuit (3DIC), multiple active layers are stacked vertically to make a single chip
- Why 3DIC? High device density, smaller chip footprint, shorter interconnects, heterogeneous integration, chip security, etc.
- Tiers are interconnected using 3D-vias. A face-to-face (F2F) bonded 3DIC uses bondpoints (micro-bumps) to interconnect the tiers, while through-silicon-vias (TSVs) are used as 3D-vias that tunnel through the active layer of a tier in face-to-back (F2B) and back-to-back (B2B) bonding



Motivation

- Several previously developed models estimate 3DIC average wire length using a Rents rule based approach, but they are lacking in the following ways:
  - Either consider a fixed size or ignore the space occupied by TSVs in active area
    - Aspect ratio of TSVs is critical for achieving acceptable yield, and due to wafer/die thinning issues, the result is a TSV that is larger compared to gates
    - As transistor sizes scale down, gates become smaller, but the size of TSVs may not scale down at the same rate
    - Hence, the estimation model must accommodate variable relative TSV sizes
  - Assume that all tiers of a 3DIC have same Rents parameters
    - 3DIC has the ability to stack diverse circuitry, like memory on logic or network-on-chip over processing cores, where all tiers may not have the same Rents parameters
    - 2DIC architecture may be modified to take full advantage of a 3DIC using a Deisgn-for-3D approach, where the Rents parameters can potentially be different for each tier
- Rents rule: An empirical relationship between the number of I/O terminals T, and the number of gates N, in a random logic network, which is expressed as:

$$T = kN^p$$

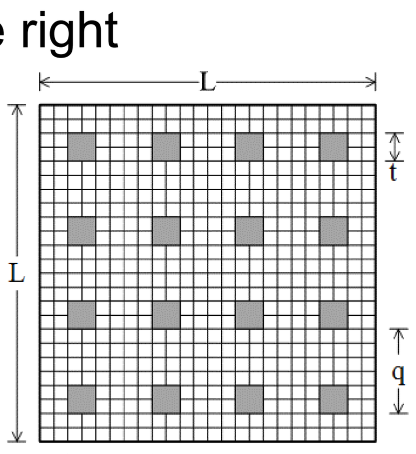
  - Where, k and p, are *Rent coefficient* and *Rent exponent,* respectively
- To enable different Rents parameters for 3DIC tiers, a tier-by-tier approach that also allows for variable TSV sizes is introduced for achieving wire length estimates in 3DICs

Tier-by-Tier Hierarchical Approach

- Using Rents rule for a logic circuit with N gates, the number of interconnects of length l, $I(l)$, is estimated [Davis *et. al.*; ITED 1998]
  - Using $I(l)$, average wire length of a 2DIC is estimated as shown below, where l_{max} is the maximum possible net-length in the circuit

$$AW_{2D} = \frac{Total\ Wire\ Length}{Total\ Number\ of\ Nets} = \frac{\sum_{l=1}^{l_{max}} l\, I(l)}{\sum_{l=1}^{l_{max}} I(l)}$$

- In a 3D-IC, TSVs occupy active-area as shown on the right
  - The dimensions are in gate-pitches
  - Each grid-box in the figure is a socket of one-gate size
  - A tier with N gates and n TSVs, with L x L size is shown
  - q is pitch of the TSVs placement, each TSV of size t x t
  - Presence of TSVs complicates $I(l)$ estimation
  - Maximum possible length is $(2L - 1)$



- In i-th tier of a 3DIC, the distribution of interconnects between *gates only*, $I_i(l)$ is estimated, then 3DIC average wire length is given by
  - N_{tiers}: # of tiers ▪ $P(i)$: wire length required for bonding i-th and $(i+1)$-th tiers
  - fo: Average fan-out ▪ $n(i)$: Number of signals between i-th and $(i+1)$-th tiers

Total wiring required for connections between gates only

$$AW_{3D} = \frac{\left[\sum_{i=1}^{N_{tiers}} \sum_{l=1}^{L_i} l\, I_i(l)\right] + \left[\sum_{i=1}^{(N_{tiers}-1)} P(i)\right]}{\left[\sum_{i=1}^{N_{tiers}} \sum_{l=1}^{L_i} I_i(l)\right] + fo\left[\sum_{i=1}^{(N_{tiers}-1)} n(i)\right]}$$

Total number of connections between gates only

Total wiring required to interconnect all pairs of adjacent tiers

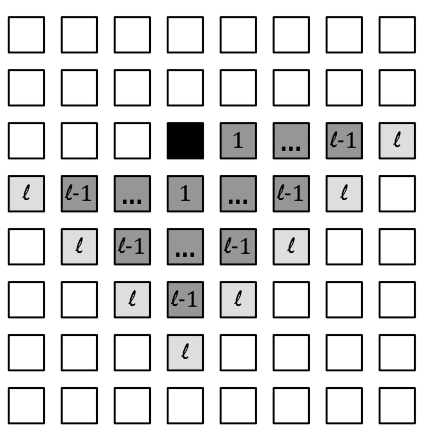
Total number of interconnects between all pairs of adjacent tiers

Impact of TSV Instances

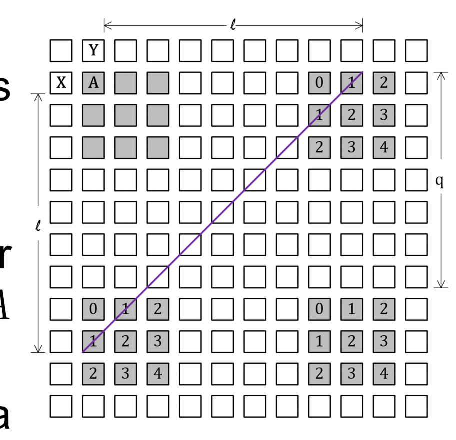
- Wire length distribution $I(l)$ is achieved by deducing $I_{exp}(l)$, the expected number of interconnects between gates separated by length l, and counting the total number of gate pairs $M(l)$ separated by length l

$$I(l) = Iexp(l)M(l)$$

- Uniform distribution is assumed for TSVs placement
- $I_{exp}(l)$ is obtained by using Rents rule and principle of conservation of I/O terminals [Davis *et. al.*; ITED 1998]
  - In 2DIC, using Rents rule, the number of point-to-point interconnects between the black socket and light-gray sockets at distance l is obtained, dividing it by number of sockets on periphery gives $I_{exp}(l)$. In 3DIC, some of these sockets are occupied by TSVs in a 3DIC tier, hence excluded for estimating $I_{exp}(l)$



  - In a given area, $(nt^2/(N+nt^2))$ of sockets are TSVs
  - Figure on the right shows the way number of sockets on periphery that are occupied by TSVs is identified
  - Value shown in each of gray sockets is $m = (l \bmod q)$
  - As m increases the number of sockets of a particular TSV that are on the periphery of radius l from A increases linearly from 1 to t, and then reduce to 0
  - A semicircle will encounter $(2\lfloor l/q \rfloor + 1)$ TSVs over a perimeter of $2l$
    - Using the two approximations $I_{exp}(l)$ is obtained



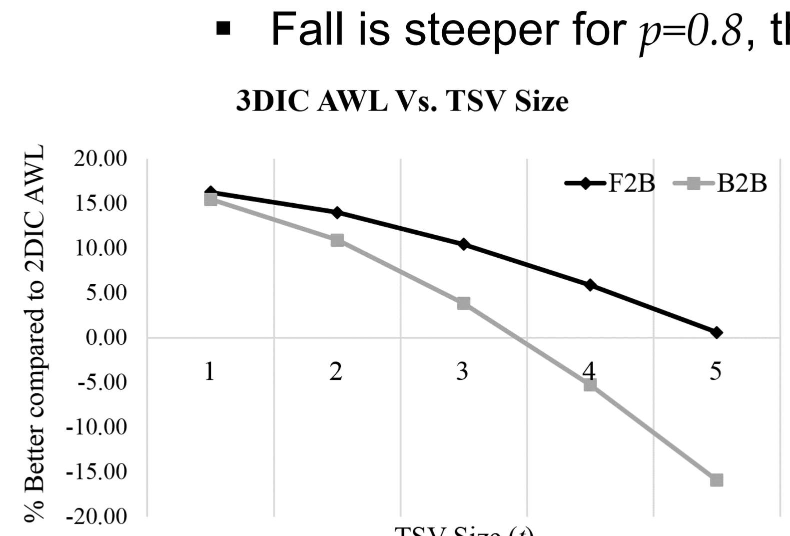
  - $M(l)$ for a tier with TSVs is obtained by counting all socket pairs separated by distance l and then subtracting TSV-to-TSV and TSV-to-gate pairs from it
- Wiring penalty between two bonding tiers

$$P = n\,[h + (fo + 1)d_{gt}]$$

  - Where n is the number of 3D-vias between the bonding tiers, h is the height of the 3D-vias (0 for bondpoints, and for TSVs the target technology determines the value), and d_{gt} is average distance between 3D-via to a gate it connects
    - For experiments d_{gt} is set to as average wire length of corresponding 2DIC
- Upper bound on number of TSVs (N_{TSV})
  - N_{TSV} is obtained by sweeping n over a large range, and identifying the point where 3DIC average wire length is more than that of a 2DIC

Results

- 3 experiments were conducted to demonstrate the utility of the model
  - A 2-tier 3DIC configuration is used for easier understanding
  - However, the model is applicable to a 3DIC with any number of tiers
  1. A circuit with 10M gates; k=4 and p=0.75, and fo=3 was used
     - Tested for three different TSV sizes (txt) , and for both F2B and B2B bonding
     - Upper bound (N_{TSV}) is found and the results are presented in the table below
     - n is set as 100,000 to compute 3DIC average wire length (AWL), and then compared to AWL of a 2DIC (Column "*% Better*" shows the comparison)
  2. Sensitivity to p: Changed to 0.74 in one of the tiers
     - 3DIC AWL in column '*AWL Diff-p*'
     - Small change in p has significant effect on 3DIC AWL, up to 5% lower
  3. Sensitivity to TSV size: 20M gates; 400,000 TSVs; k=4, p=0.8, and fo=3
     - TSV dimension t was swept from 1 to 5 (see graph below)
     - Steep fall in performance compared to 2DIC as t increases indicates that TSV size becomes extremely crucial in circuits with large numbers of interconnects
     - Fall is steeper for p=0.8, than that for p=0.75 in the first experiment



N = 10,000,000		n = 100,000			
Bonding	*t*	N_{TSV}	*AWL*	*% Better*	*AWL Diff-p*
F2B	2	788700	26.36	13.44	25.34
B2B	2	406000	26.92	11.61	25.84
F2B	3	430300	26.95	11.50	25.95
B2B	3	205200	28.10	7.74	26.97
F2B	4	264700	27.73	8.94	26.77
B2B	4	124000	29.67	2.58	28.48

Conclusions

- A tier-level hierarchical approach based on Rents rule is introduced for estimating 3DIC average wire length
  - Discrete wire length distribution of each tier is estimated independently to provide the ability to handle tiers with different Rents parameters
  - Applicable for variable TSV dimensions and for all bonding techniques
  - Using the model, the upper bound on the number of TSVs is attained
- Future work: Model will be further validated against 3DIC designs and will be used to estimate other performance metrics