USC University of Southern California

USC Viterbi School of Engineering

Ming Hsieh Department of Electrical Engineering

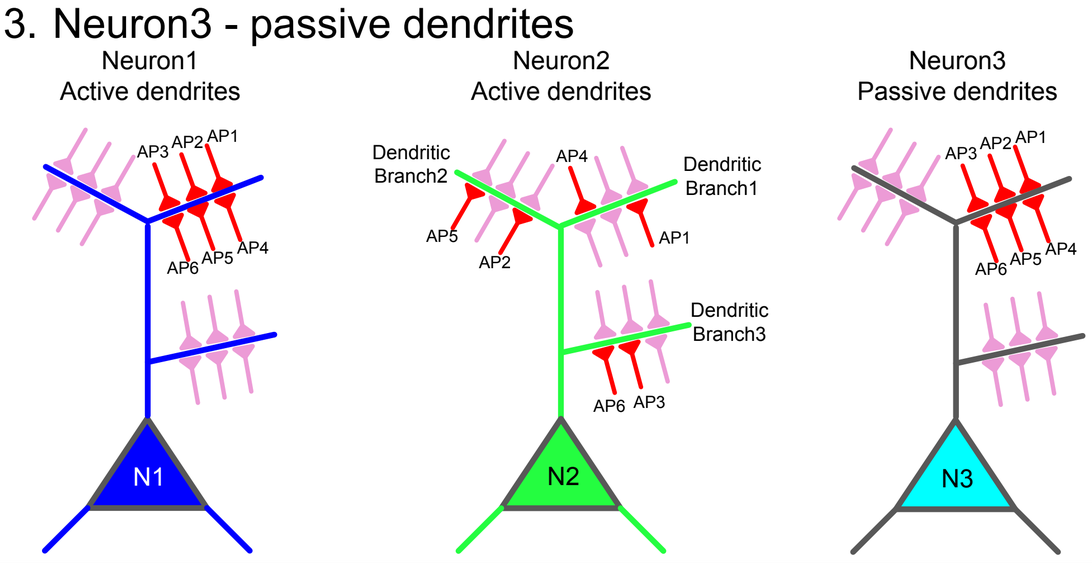
Dendritic Spike-Evoked Precise Neuronal Firing Timing in Neuromorphic Circuits

Chih-Chieh Hsu and Alice C. Parker

BioRC Group, Ming Hsieh Department of Electrical Engineering, University of Southern California

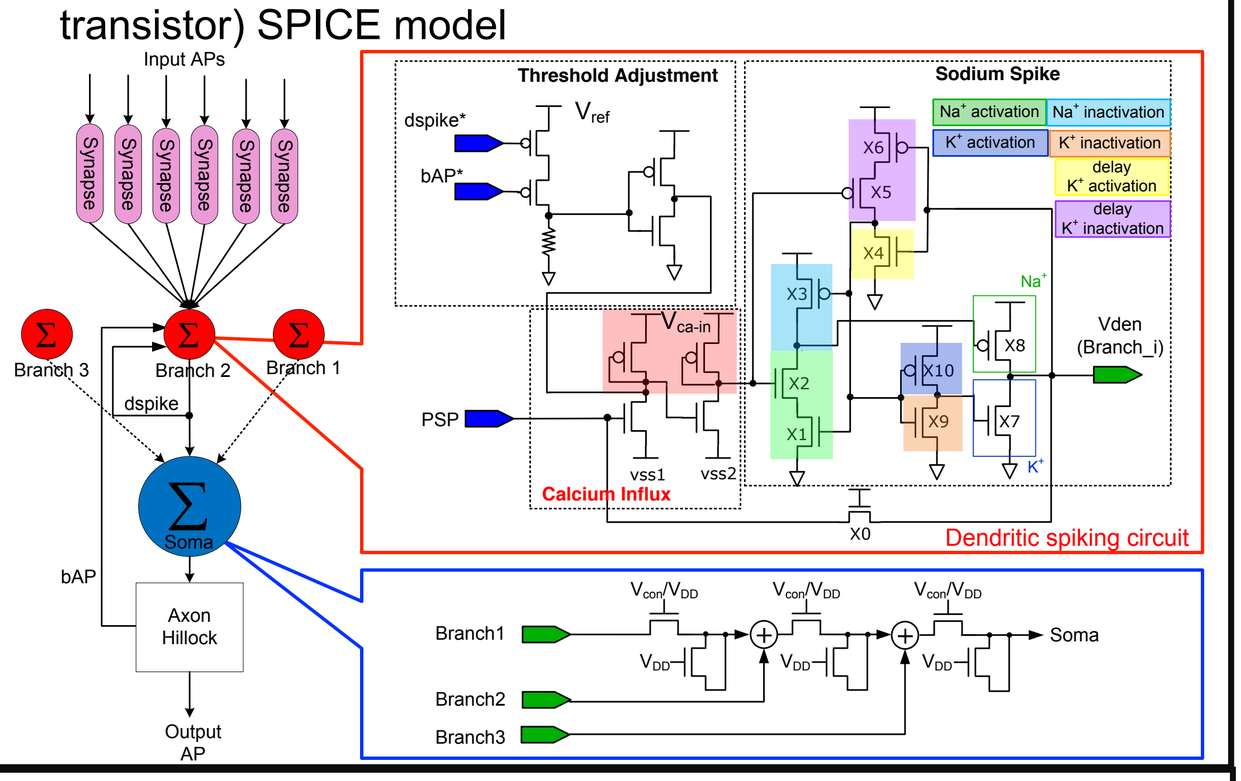
Motivation & Introduction

- The biological neuron has *complex* and highly *nonlinear* dendritic computations – dendritic spiking
- These dendritic spikes are key to initiate precisely timed axonal AP (action potential) and hence empower the input-output transformation among neurons
- Three model neuron configurations:
  1. Neuron1 - clustered synapses onto same branch
  2. Neuron2 - distributed synapses on different branches
  3. Neuron3 - passive dendrites



Model Neuron Setup

- Each model neuron has circuit components: 18 synapses, 3 dendritic branches, soma, and axon hillock (~300 transistors)
- Non-linear two-stage dendritic arbor implemented
- Circuit designed using CNFET (carbon nanotube field-effect transistor) SPICE model

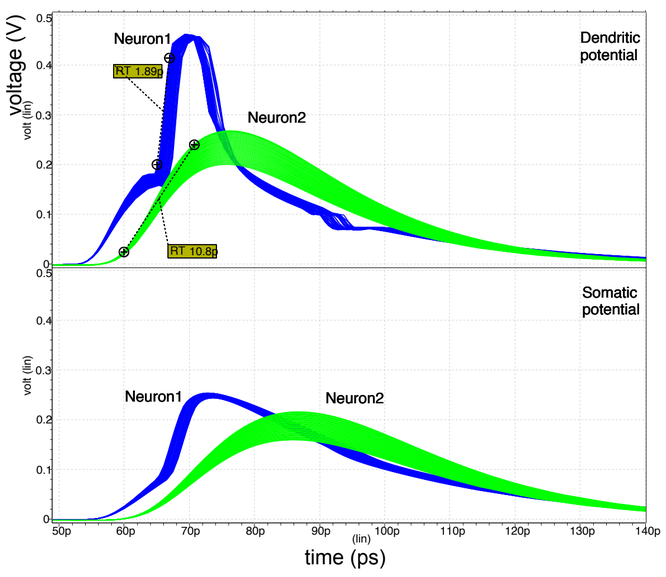


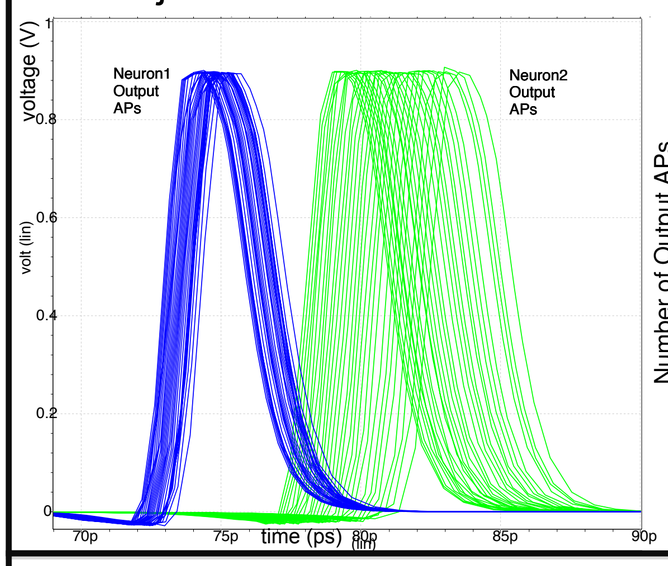
CNFET Simulation Results

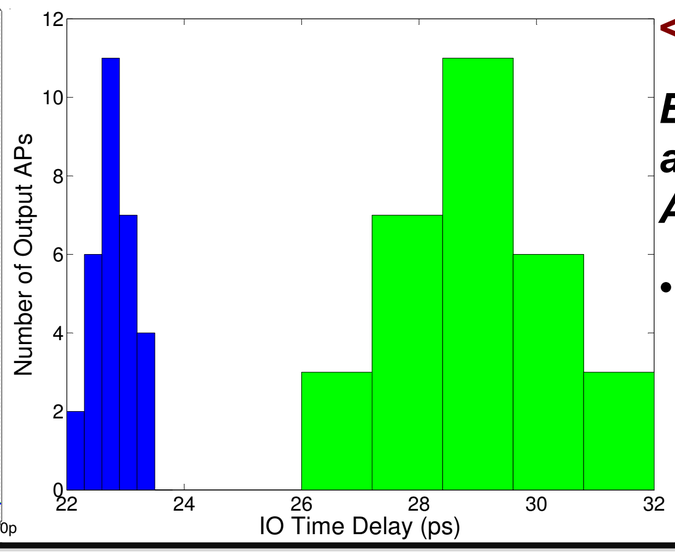
< Experiment I >

Effect of dendritic spike on output AP timing

- Dendritic spike (Neuron1) leads to larger dv/dt in the somatic potential compared to PSP alone (Neuron2)
- Large dv/dt in the somatic potential results in relatively invariant IO delay and less AP jitter



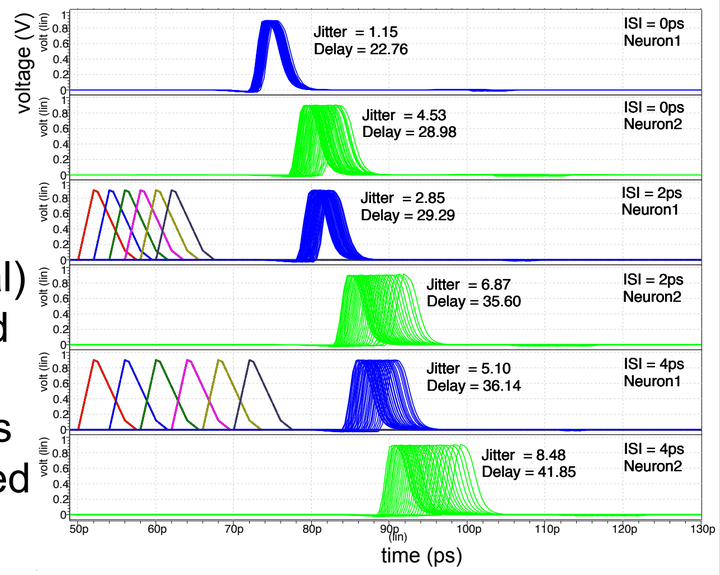




< Experiment II >

Effect of synaptic synchronization on output AP timing

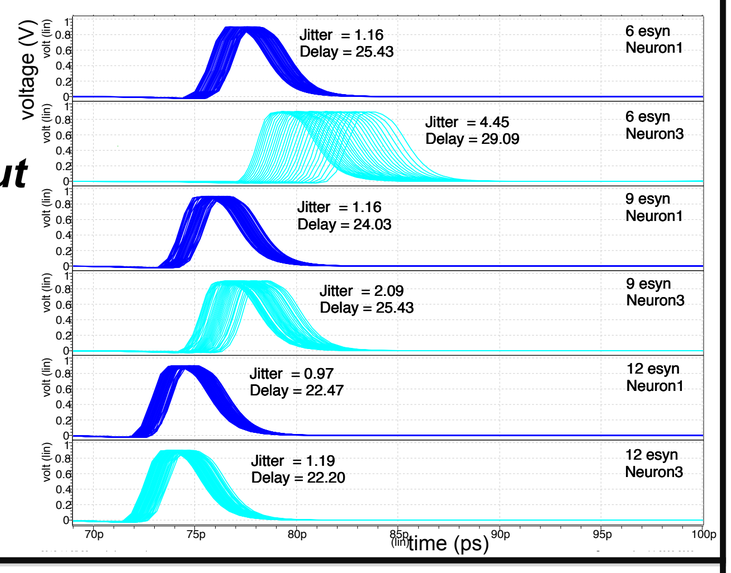
- ISI (inter-stimuli interval) between inputs AP_i and AP_{i+1} varies
- Dendritic spike requires spatiotemporal clustered inputs



< Experiment III >

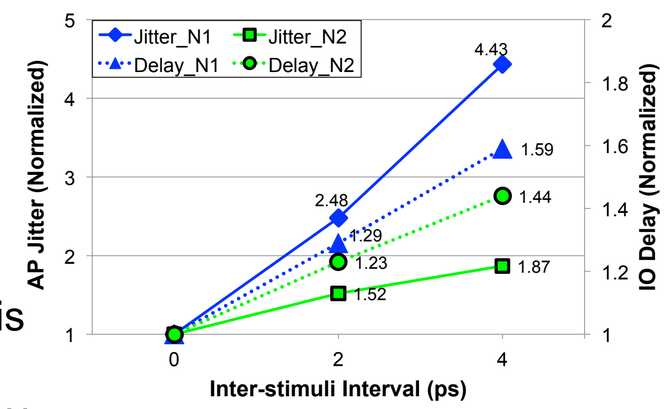
Effect of synaptic activation level on output AP timing

- Number of synapses activated in Neuron1 and Neuron3 varies

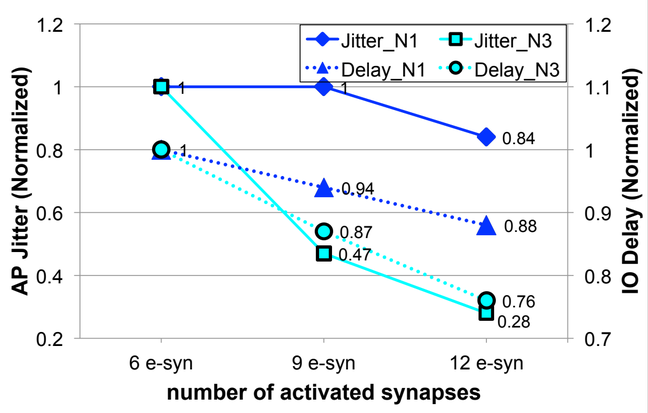


Results and Discussion

- When ISI increases, output AP jitter and IO delay in both model neurons increase
- The rate of increase is higher in Neuron1 because dendritic spike is more sensitive to the degree of input synchrony



- When the active dendrites are absent (Neuron3), the AP jitter and IO delay are highly dependent on the number of synapses activated
- With passive dendrites only, it would require more neurons to achieve accurate signal transformation



Ming Hsieh Institute

Ming Hsieh Department of Electrical Engineering