



Toward Separated Carbon Nanotube Based Large Scale Thin-Film CMOS Integrated Circuits



Jialu Zhang[†], Chuan Wang[†], Yue Fu, and Chongwu Zhou

Dept. of Electrical Engineering, University of Southern California, jialuzha@usc.edu

[†] These authors contributed equally to this work

Introduction

Flexible transparent thin-film transistors are important for applications such as flat-panel displays, e-papers and radio-frequency identification tags. However, the challenge is to find the right channel materials.



Materials	Advantages	Challenges
α -Si TFTs	- High Reliability - Presently used in LCDs	(a) High temperature processing; (b) Low mobility ($\mu \leq 1 \text{ cm}^2/\text{V}\cdot\text{sec}$)
Poly-Si TFTs	- High mobilities ($\sim 150 \text{ cm}^2/\text{V}\cdot\text{sec}$) - Presently used in AMOLEDs	(c) High temperature processing; not suitable for plastic substrates
OTFTs	- Low temperature processing: - can use on plastic substrates	(d) Low mobilities ($\mu \leq 1 \text{ cm}^2/\text{V}\cdot\text{sec}$) (e) Moisture sensitivity

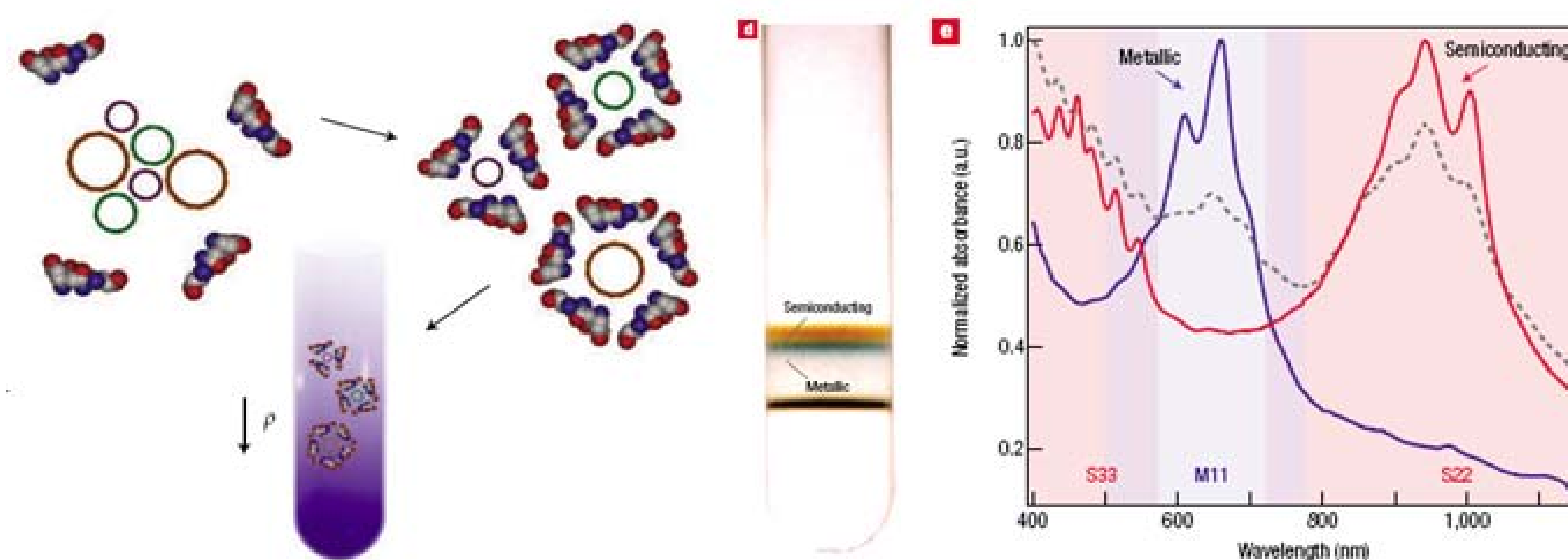
Carbon nanotubes: Significantly higher mobility, compatible with transparent flexible electronics, low temperature processing: low cost.

Challenges: 1. Coexistence of metallic and semiconducting nanotubes.
2. Carbon nanotubes are usually p-type doped in ambient air.

Experimental

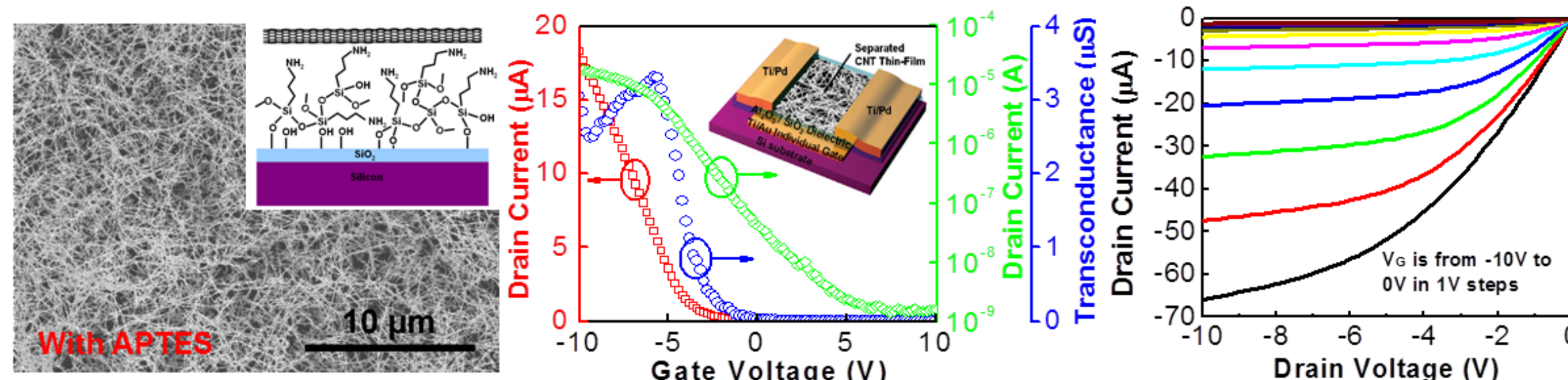
Separation of metallic and semiconducting nanotubes:

Density gradient ultracentrifugation method



M. Arnold, M. Hersam et al., *Nature Nanotechnol.*, Vol. 1, 60, 2006

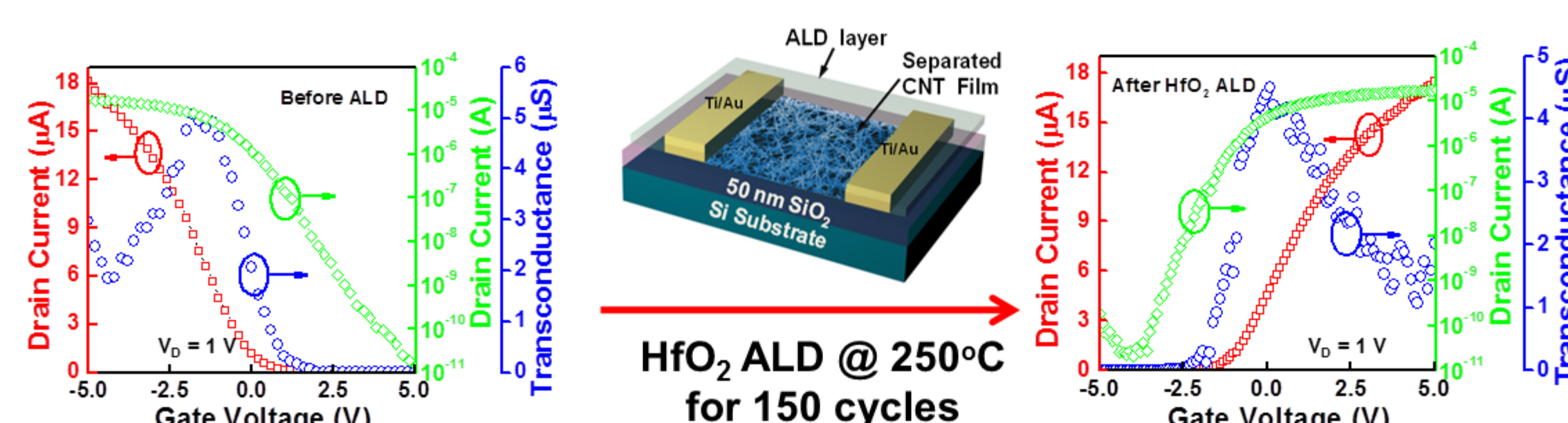
p-Type thin-film transistors:



- 95% semiconducting nanotube solution
- On/off ratio: ~ 10000 , peak transconductance: $3.5 \mu\text{S}$
- Highest mobility of $67 \text{ cm}^2/\text{V}\cdot\text{sec}$

n-Type thin-film transistors:

By passivate the p-type SN-TFTs with high- κ oxide layer using atomic layer deposition (ALD), the transistors are converted to n-type

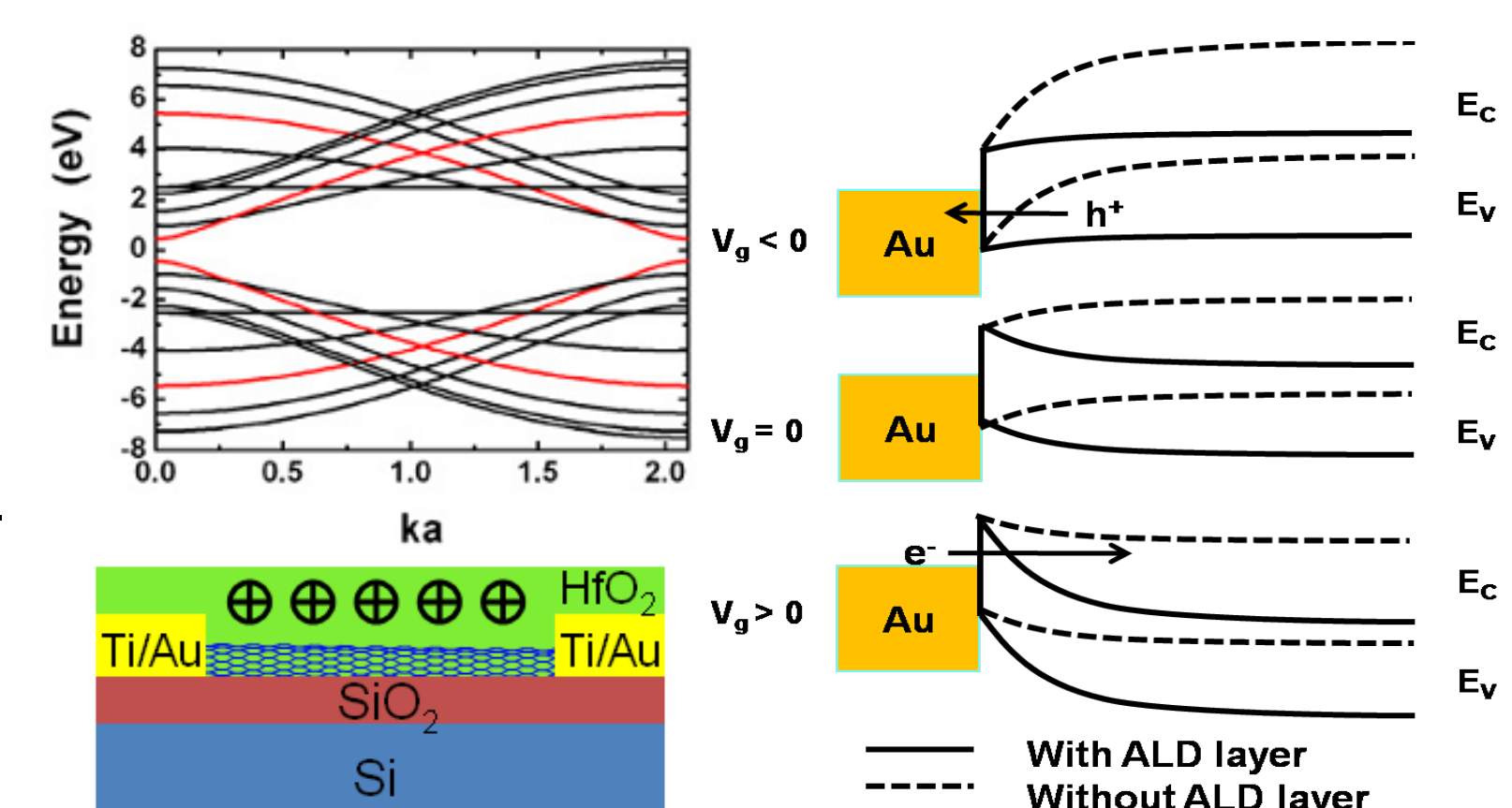


	On-current	transconductance	On/off ratio	Device mobility
Before ALD	18.1 μA	5.06 μS	1.616×10^6	$5 \text{ cm}^2/\text{V}\cdot\text{s}^{-1}$
After ALD	17.4 μA	4.59 μS	1.34×10^6	$3 \text{ cm}^2/\text{V}\cdot\text{s}^{-1}$

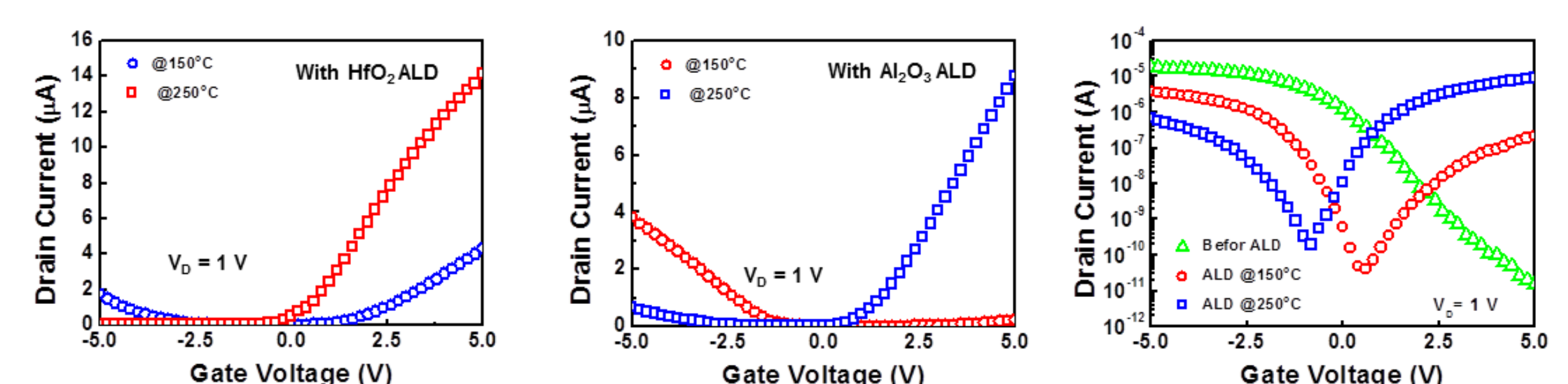
In-depth study of n-type SNTFTs

Mechanism of the Carrier conversion:

- Symmetric E-k relationship for holes and electrons
- The baking process in the vacuum chamber during ALD drives away O_2
- Positive fixed charge in the high- κ oxide layer introduced due to the deficiency of oxygen atoms will tune the energy band



ALD temperature dependence:

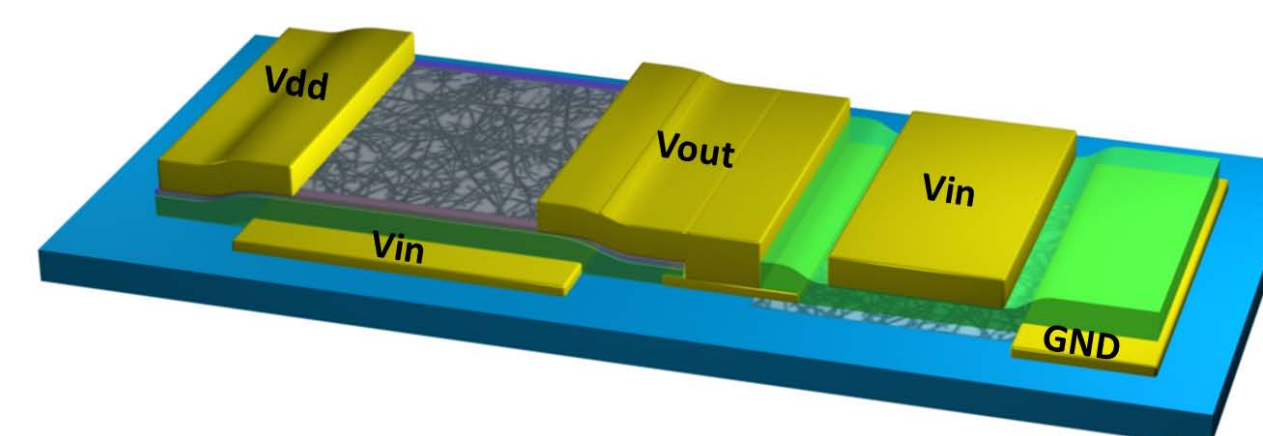


@250 °C (compared with 150°C)

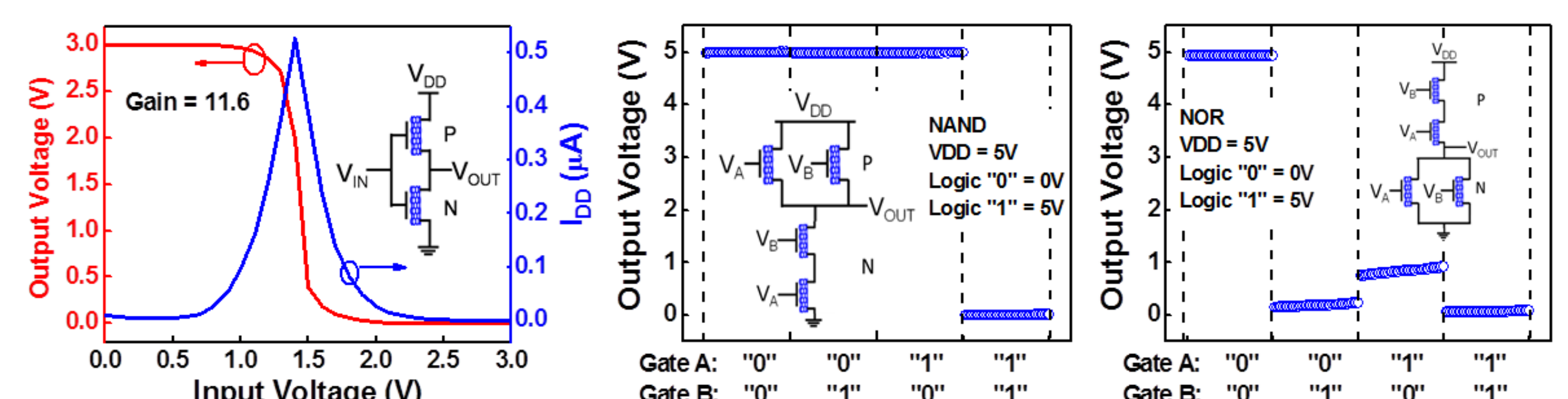
- H_2O vaporizes **faster** and is pumped away immediately
- **Less oxygen atoms** available during the formation of high- κ oxide layer.
- **More positive charge** is accumulated and the nanotube energy band will be **bent down** even further.

Applications

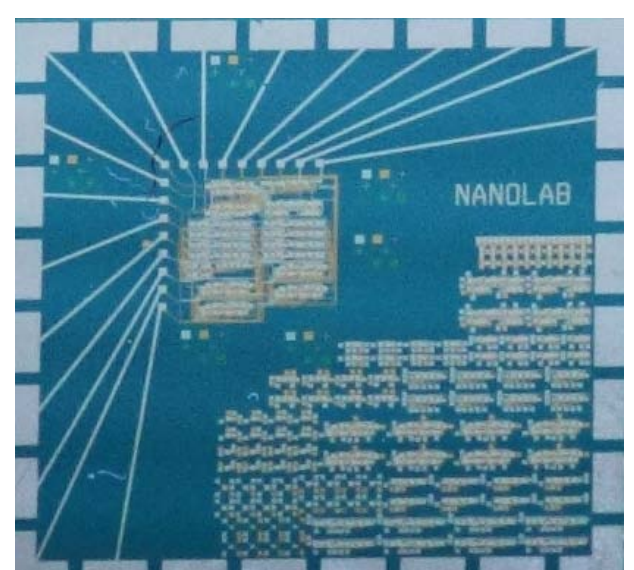
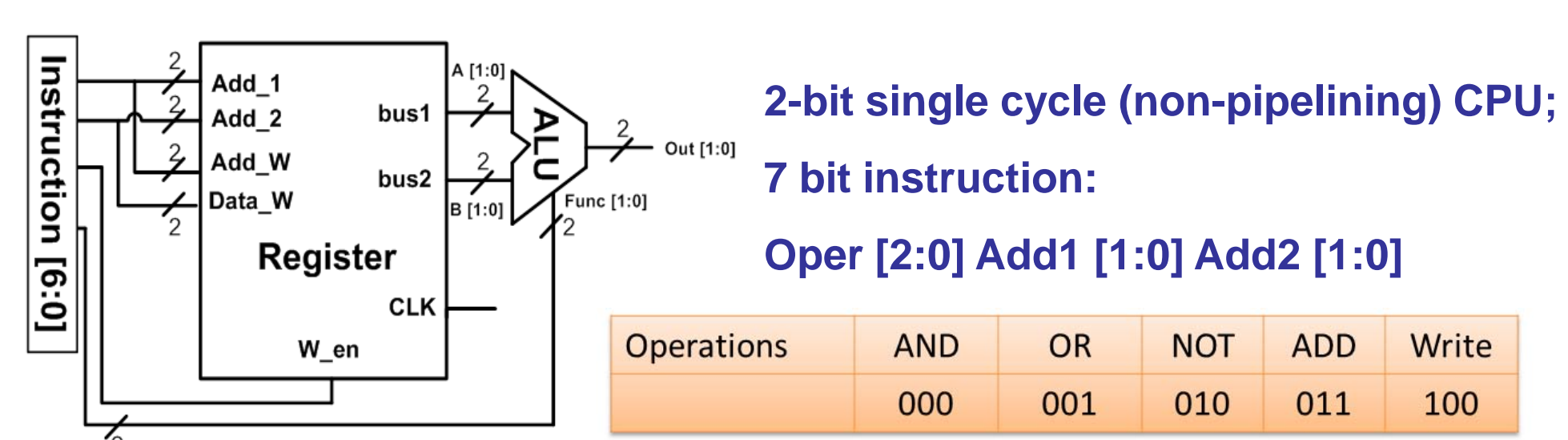
CMOS integrated logic gates:



We use back-gated structure for p-type SN-TFTs and top-gated structure for n-type SN-TFTs and integrate them together for CMOS circuits



2-bit CMOS CPU (ongoing):



Conclusion

We have developed a platform for high performance n-type and p-type separated nanotube TFTs with high yield. Devices exhibit significantly better performance compared with state-of-the-art amorphous silicon and organic TFTs. Our work represents significant advance toward the challenging tasks such as nanotube separation, assembly, air-stable n-type device fabrication and can provide guidance to future research on SN-TFT based large scale CMOS integrate circuits.

Chuan Wang[†], Jialu Zhang[†], Chongwu Zhou, et al., *Nano Letters*, Vol. 9, pp. 4285-4291, (2009)

Chuan Wang[†], Jialu Zhang[†], Chongwu Zhou, et al., *ACS Nano*, Vol. 4, pp. 7123-7132, (2010)

Jialu Zhang, Chuan Wang, Chongwu Zhou, et al., *ACS Nano*. ASAP, (2011)



UNIVERSITY OF SOUTHERN CALIFORNIA