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A 95-MS/s 11-bit 1.36mW Asynchronous SAR ADC with Embedded Passive Gain in 65nm CMOS

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Motivation

Conventional ADC Architecture Analysis:

1. Synchronous SAR ADC

2. Asynchronous SAR ADC

- Advantages
  - Power efficient topology
  - Scaling Friendly architecture
  - Speed up by asynchronous clocking

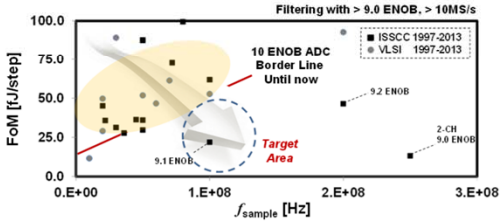
3. Pipelined SAR ADC

- Advantages
  - Relaxed sub-ADC's spec. (Mainly each comparator)
  - Enhanced speed from pipelined operation
- Disadvantages
  - Active Amp: Power dissipation ↑
  - Passive Amp: Distortion ↑ due to non-linear parasitic cap (∵ Open-loop circuit)

Objective: Find out the best power efficient ADC architecture in high-speed and high-resolution regimes.

State-of-the-art

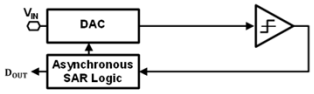
Applications: Future Mobile Communication Devices



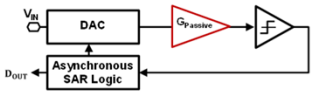
- **Requirement for the target region**
  - Significantly power constrained with high dynamic range

Proposed Asynchronous SAR ADC

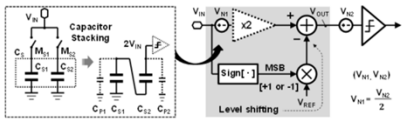
- **Traditional Asynch. SAR ADC**



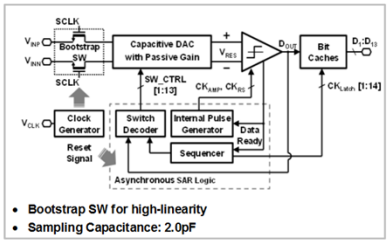
- **Proposed Asynch. SAR ADC**



- **Basic concepts for Passive Gain stage**

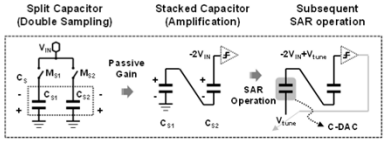


- **Entire block diagram**

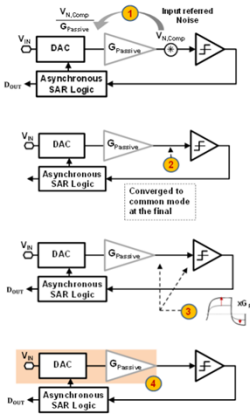


- Bootstrap SW for high-linearity
- Sampling Capacitance: 2.0pF

- **Basic operating sequences**



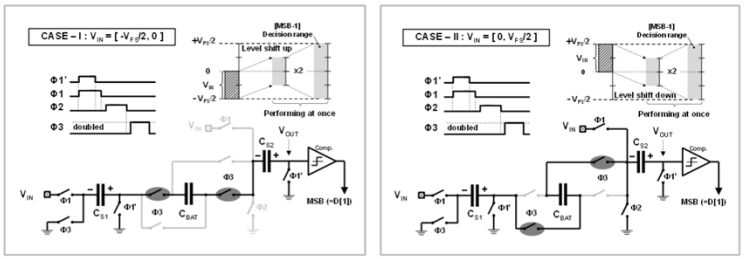
Key Highlights



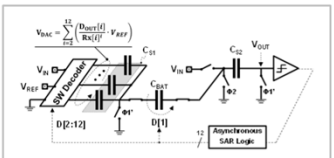
- **Passive amplifier(Power-less)**
  - ► Comparator noise requirement ↓
- **Redundant SAR operation**
  - ► Non-linear distortion effect ↓
- **Passively amplified signal**
  - ► Comparison time ↓
- **Embedding $G_{Passive}$ into DAC**
  - ► DAC settling time ↓
  - ► Rail-to-Rail input swing

Integrated Circuit Implementation

Proposed level shifting circuit to prevent voltage over-range issue

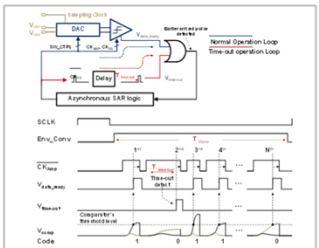


Subsequent SAR circuits

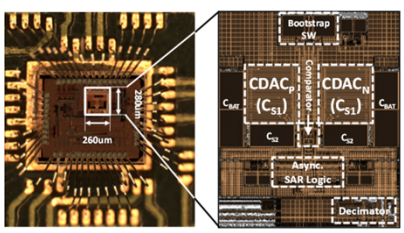


- Non-binary weighted CDAC (C_{S1})
- Small sized NMOS with doubled clocking for intermediate switches
- Sufficiently large size of C_{BAT} (4pF) to mitigate leakage problem

Time-out Scheme



Chip Photograph



Active area = 0.073mm²

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IEEE CICC 2013 [Accepted]

Measurement Results & Performance Summary

Static performances

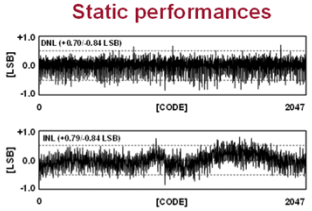
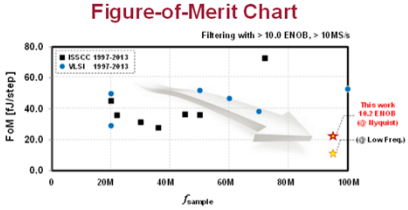
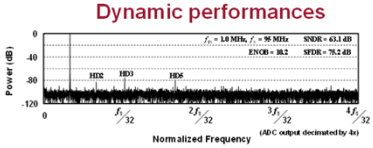


Figure-of-Merit Chart



Dynamic performances



*"Proposed **Embedded Passive Gain technique** enhances conventional Asynchronous SAR **ADC structure's Power Efficiency** in high resolution regime."*

ADC Topology	Asynchronous SAR with Passive Gain
$f_{sampling}$	95-MS/s
Resolution	11-bit
Signal Bandwidth	47.5 MHz
Supply (V)	1.1 V
SFDR (dB)	75.2 dB
SNDR (dB)	63.1 dB
Power (mW)	1.36 mW
Area (mm²)	0.073 mm²
Process (nm)	65 nm CMOS
FoM	22 fJ/conv.-step

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