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Neural Stimulating CMOS Chip

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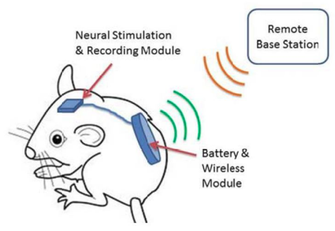
Motivation

Develop a fully implantable bioelectronics system, capable of interfacing with neural systems in a bidirectional manner (recording and stimulation), specifically for log-term, free-roaming, small animal neuroscience research.

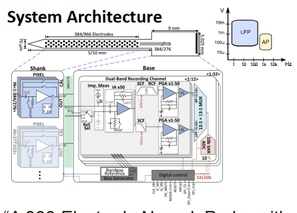
The implantable system includes a multi-electrode neural stimulating and recording CMOS integrated circuit with wireless power and data telemetry capability (Prof. Hashemi's group), parylene microelectrode arrays (Prof. Meng's group), and other necessary components in a proper package (Prof. Weiland's group). The envisioned experiments using this platform by neuroscientist collaborators (Prof. McGee's and Prof. Berger's groups) include experiments in visual cortex plasticity, experiments in visual mid-brain plasticity, and hippocampal studies to identify neural behaviors of untethered animals in complex environments.



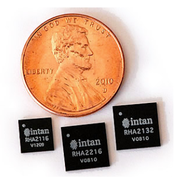
State of the Art

- Single- and multi-electrode neural stimulating integrated circuits, realized in CMOS, have been reported by research groups and are offered by companies (e.g., Intan Technologies).

x Shortcomings of the existing solutions
  - Power inefficient



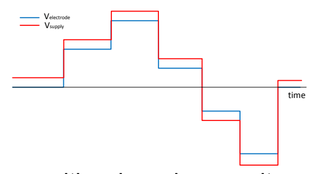
"A 966-Electrode Neural Probe with 384 Configurable Channels in 0.13μm SOI CMOS", C. M. Lopez, et al., IMEC. ISSCC 2016



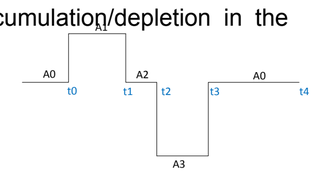
Intan Technologies amplifier

Innovative Approaches & Design Features

- Adjust the level of DC power supply of the current stimulator as a function of stimulating current to ensure a low dropout voltage across stimulating devices and maintain high efficiency across a wide range of stimulating current and load values.

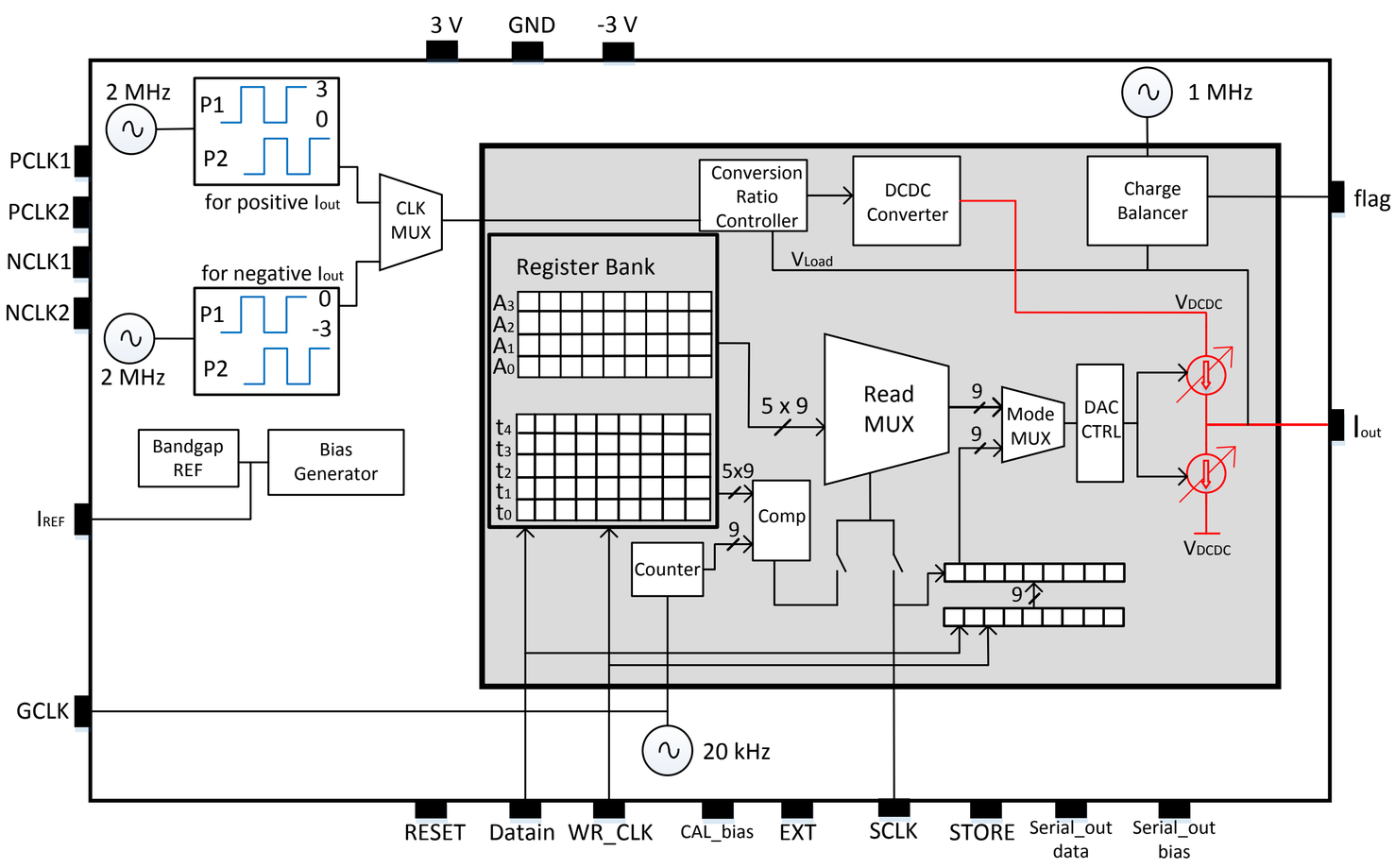


- Switched-capacitor DC-DC voltage converters with shared capacitors generate the necessary DC power supplies.
- Charge-balancer ensures zero net-charge accumulation/depletion in the tissue (load).
- Two stimulating modes:
  - (1) Pre-programmed biphasic periodic waveform with controllable pulse intervals (9 bits for each time instance t_0, t_1, t_2, t_3 and t_4) and amplitude (9 bits for each amplitude A_0, A_1, A_2 and A_3),
  - (2) Arbitrary waveform – every 50 μs a new latched pulse may be sent to the chip from an external source.



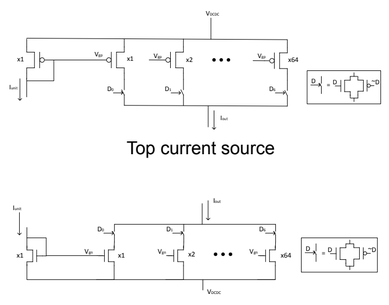
- Amplitude of the stimulating current may vary within (-100 μA, +100 μA) in 100 nA steps.
- The load can vary from a few kΩ to 40 kΩ to accommodate for different electrode sizes and implant locations.

Neural Stimulator Chip Architecture



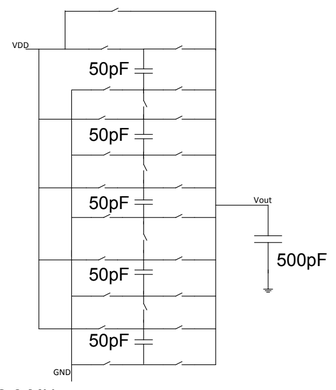
Circuit Building Blocks

Current Source Blocks



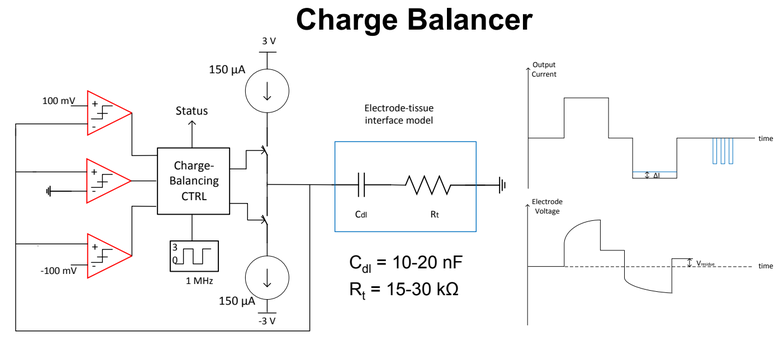
- 8 bit resolution + 1 bit redundancy
- Minimum pulse width 50 μs
- Settling time 10 μs for 90% rise/fall time

DC-DC Converter



- f_{sw} = 2-3 MHz
- Conversion ratios 5:1, 3:1, 2:1, 3:2 and 6:5
- Generating both positive and negative voltages from 3 V and -3 V voltage sources
- Efficiency > 60% (peak 85%)

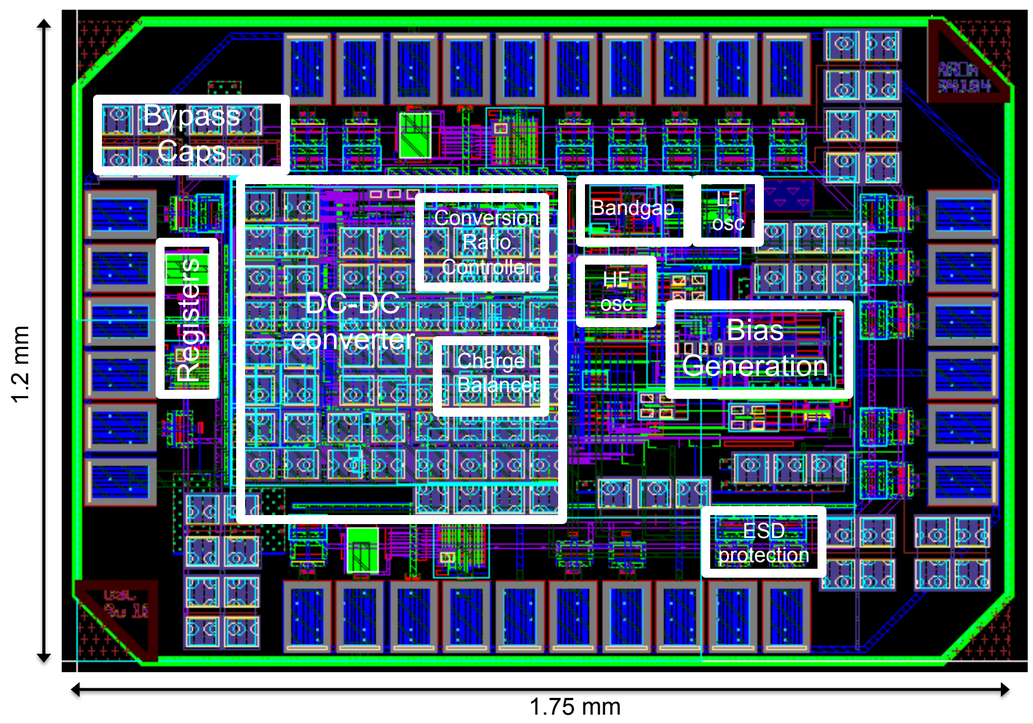
Charge Balancer



C_{dl} = 10-20 nF
R_t = 15-30 kΩ

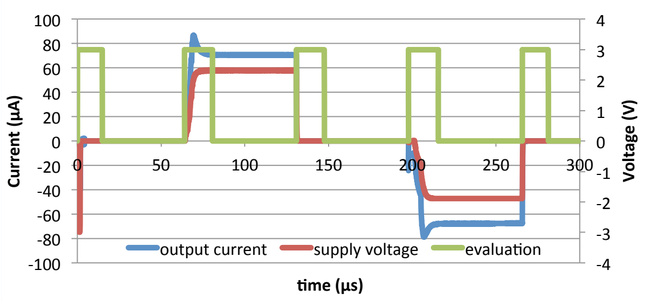
During the resting time between consecutive cycles (user controlled), short current pulses cancel any residue charge on the electrode, if the electrode voltage goes beyond the safety window.

Chip Layout (130nm CMOS)



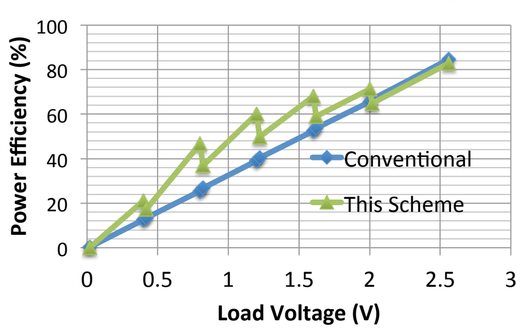
Simulated Results

Transient Waveforms



- In evaluation phase, the conversion ratio controller circuitry is on.

Power Efficiency vs. Load Voltage



Performance Summary

	[1]	[2]	[3]*	[4]**	[5]	This Work
Technology	0.18-μm SOI	0.35-μm HV CMOS	0.18-μm HV CMOS	0.35-μm HV CMOS	0.35-μm HV CMOS	0.13-μm CMOS
VDD (V)	0.8	3.3	3.3	3.3	3.3	±3
Stimulation Supply Voltage V_{Stim} (V)	-3.3 ~ +3.9	2.5-17 Programmable (3 bits) Charge Pump	7	120	75	**±0.56, ±0.94, ±1.44, ±1.9, ±2.3 Automatically Reconfigurable**
Channel Count	16	8	8	8	8	1
Max. Output Current	145 μA	310 μA	1 mA	10.24 mA	4 mA	127 μA
Output Resolution (bits)	5	10	6	8	6	7
DNL/INL (LSB)	N/A	N/A	0.16/1.25	0.19/0.16	0.4/2.2	0.6/0.6
Max Frequency (kHz)	N/A	3.3	20	N/A	2	10
Total Quiescent Power	N/A	5-29 mW	559 μW	14.4 mW	2.15 mW	32 μW
Power/channel	N/A	0.6-3.6 mW	70 μW	1.8 mW	269 μW	4 μW***
Die Size (mm^2)	9	17.68	2 (estimated)	7.1	5.94 (core)	2.1
Channel Area (mm^2)	0.56	2.21	0.25 (estimated)	0.28	0.74	0.49

* Sensor, sound processor and ADC are not included for a better comparison. ** Simulation results are reported. ***Assuming an 8 channel realization.

[1] S. Ha et al., "A 16-Channel Wireless Neural Interfacing SoC With RF-powered Energy Replenishing Adiabatic Stimulation", Symposium on VLSI Circuits Digest of Technical Papers, 2015
[2] L. Bisoni et al., "An HV-CMOS Integrated Circuit for Neural Stimulation in Prosthetic Applications", IEE Transactions on Circuits and Systems, VOL. 62, No. 2, February 2015
[3] M. Yip et al., "A Fully-Implantable Cochlear Implant SoC With Piezoelectric Middle-Ear Sensor and Arbitrary Waveform Neural Stimulation", IEE Journal of Solid State Circuits, VOL. 50, No. 1, January 2015
[4] D. Osipov and S. Paul, "8 Channel Neural Stimulation ASIC for Epidural Visual Cortex Stimulation with on Board 90 ppm/◦C Current Reference", IEEE, 2015
[5] L. Zeng et al., "A high-voltage stimulation chip for wearable stroke rehabilitation systems", International Journal of Circuit Theory and Applications, November 2015

Future Work

- Other methods to increase current source efficiency will be investigated.
- Neural signal recording system will be designed addressing 2 main challenges:
  1) Area per channel (< 40 μm x40 μm)
  2) Power per channel (< 1 μW)
- Stimulating and recording systems will be integrated on a single chip, with wireless power and data telemetry capability.

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