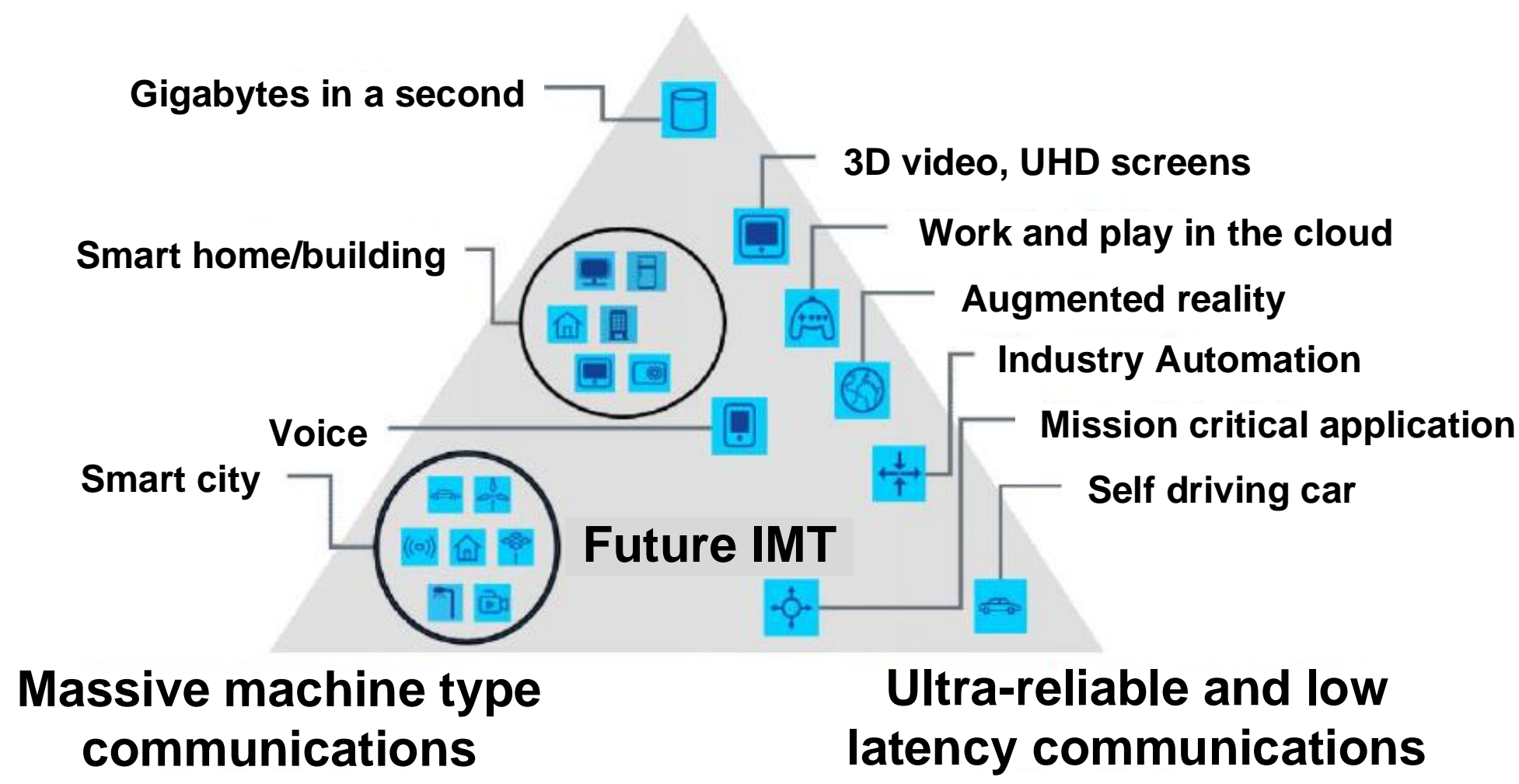


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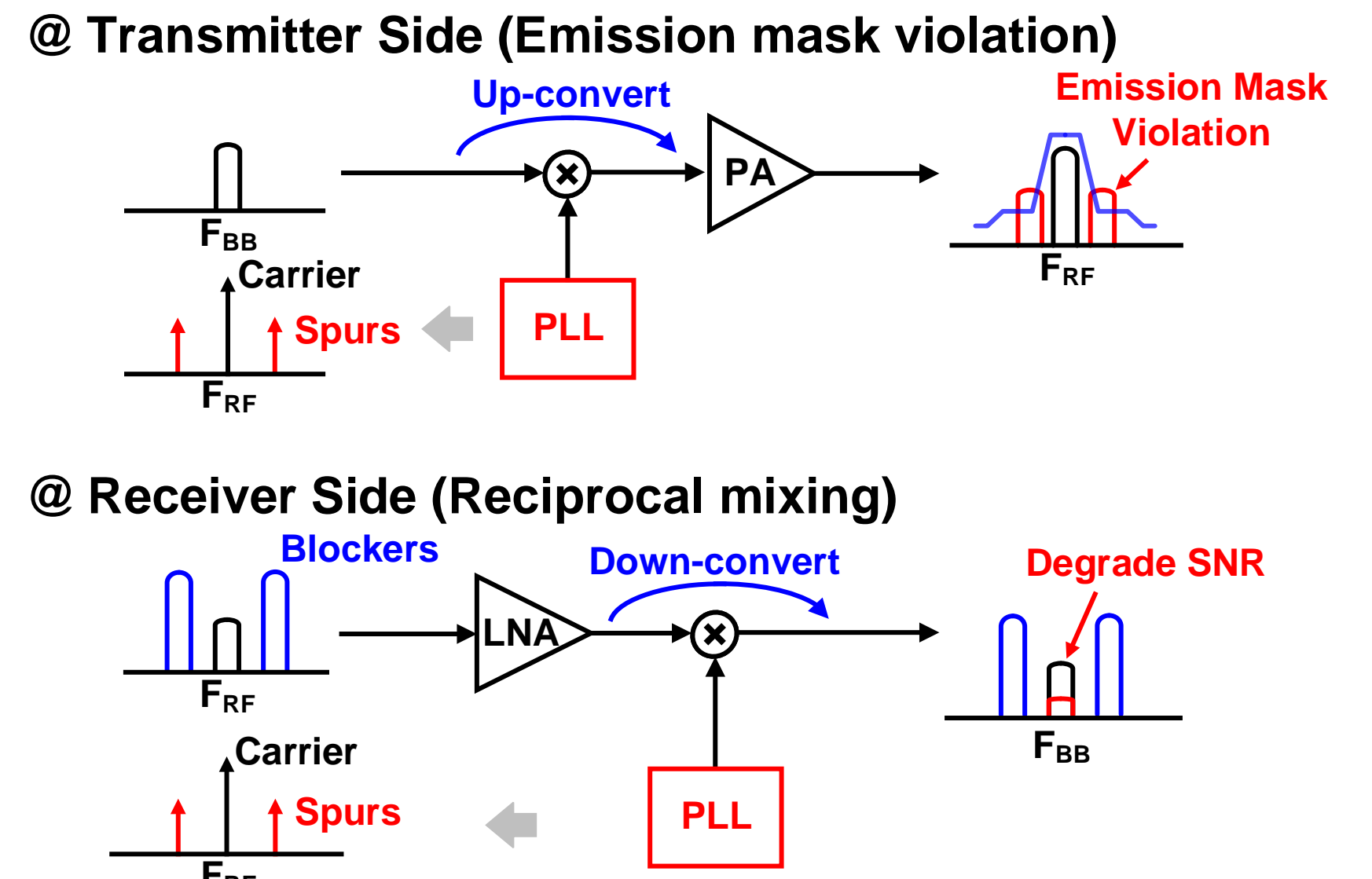
5G Communication for 2020 and Beyond

Enhanced mobile broadband [ITU-R M.2083-0, 2015]

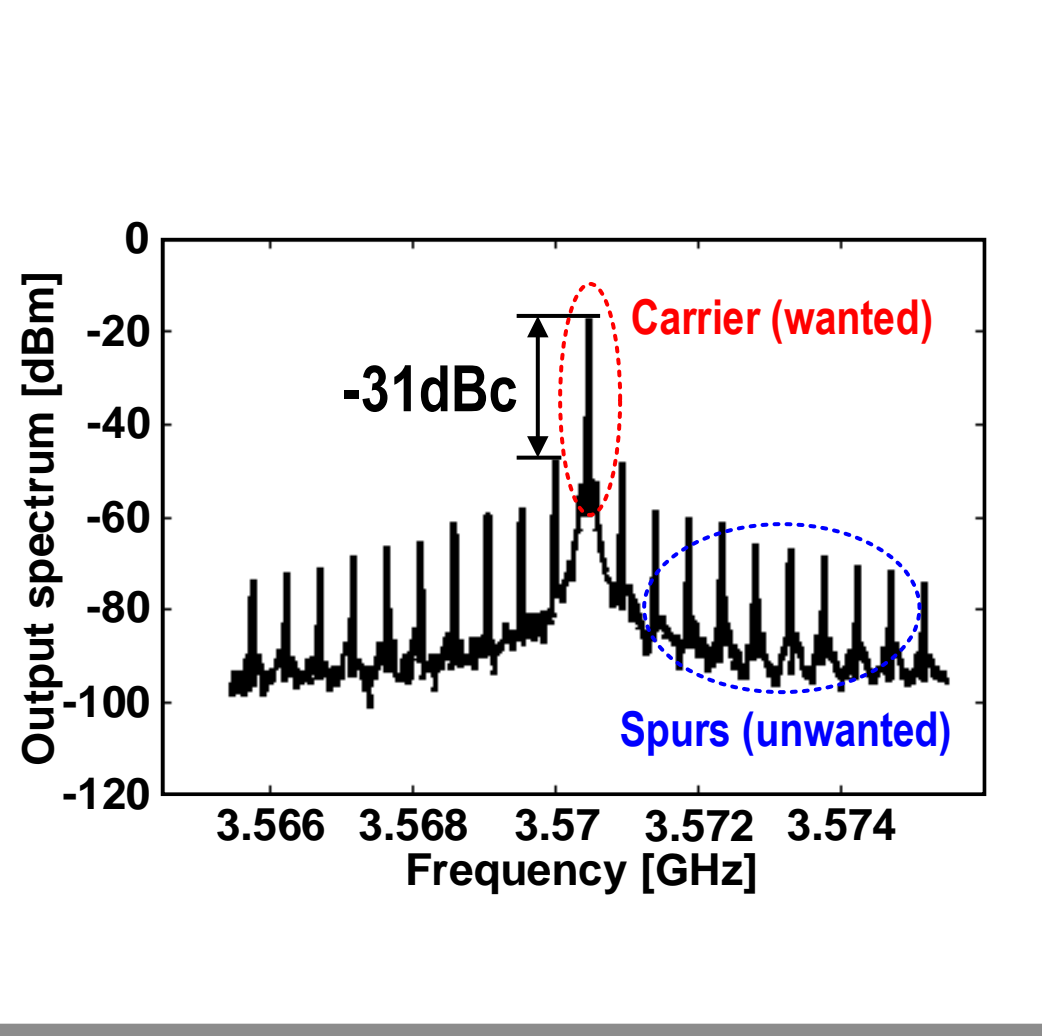


=> 5G requests low-cost and high-performance clock generator to support variety of systems.

PLL with Spurs in Wireless Transceiver



Contaminated Spectrum



Sources of Spurs

SoC Interference Coupling

DPLL Fractional-N Operation

$F_{ref} = N \cdot m \cdot F_{PLL}$

Self-Coupling

[C.R. Ho and M.S.W Chen, IEEE RFIC 2014]

Proposed Ultra-low Spur DPLL Solution

DSP-enabled Digital Phase-Locked Loop Architecture

Spur Function: $\Phi_{err}[n] = A_r \cdot \text{sawtooth}(\omega \cdot k \cdot T_s + \Phi_r)$

Cancel Function: $\Phi_{cancel}[n] = A_c \cdot \text{sawtooth}(\omega \cdot k \cdot T_s + \Phi_c)$

Direct Spur Cancellation in DSP

Chip Micrograph

[Cheng-Ru Ho and Mike Shuo-Wei Chen, IEEE ISSCC 2016]

Measurement Result and State-of-the-arts Comparison