USC University of Southern California

USC Viterbi School of Engineering

Ming Hsieh Department of Electrical Engineering

Energy-efficient Edge-centric Graph Processing on FPGA

Shijie Zhou, Charalampos Chelmis and Viktor K. Prasanna
Ming Hsieh Department of Electrical Engineering

Introduction and Background

Graph analytics is widely used in many areas

Social network

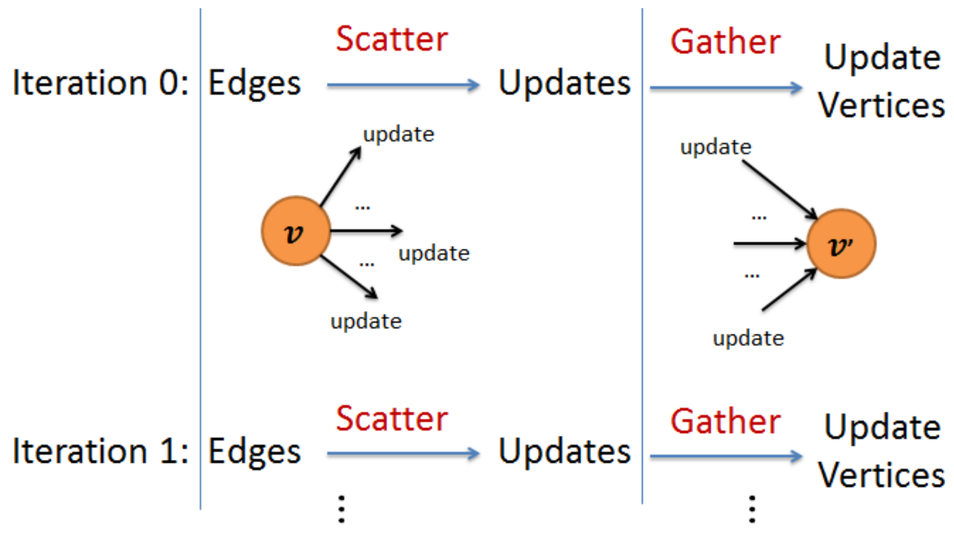
Internet

Road network

Obtaining high performance is challenging

- Massive datasets
- Poor locality of memory accesses
- High data-access-to-computation ratio

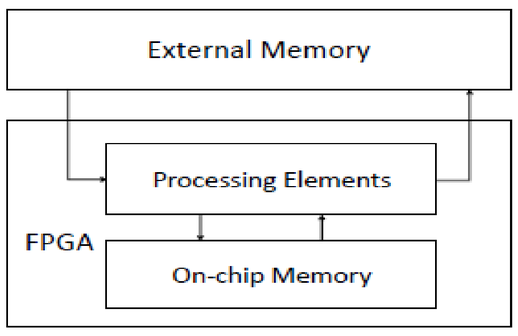
Edge-centric (gather-scatter) paradigm



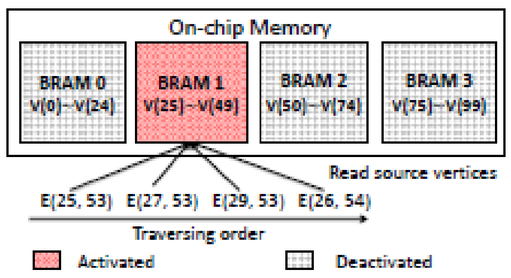
Algorithm and Optimization

Algorithm 2 Single-source Shortest Path

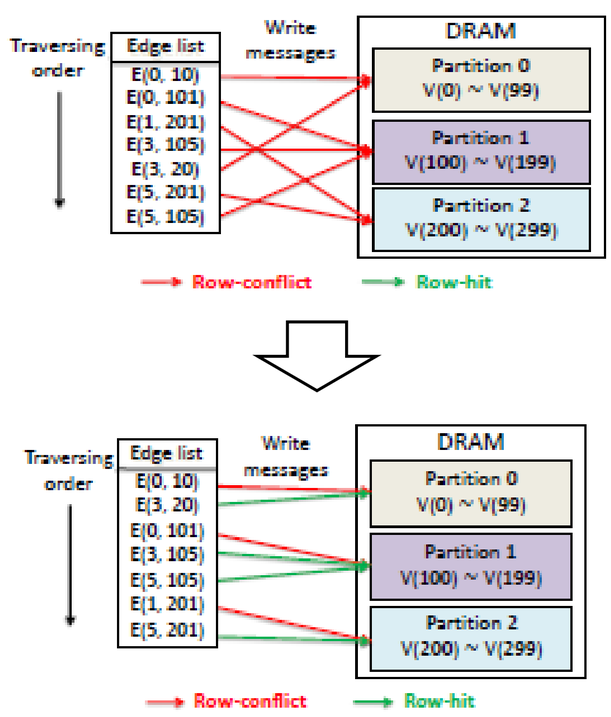
```
1: while not done do
2:    Scatter:
3:    for each partition do
4:       read vertex set from external memory and store into
         on-chip memory
5:       for each edge e in edge list do
6:          read weight of vertex e.src from on-chip memory
7:          let a = weight of vertex e.src
8:          produce an message m
9:          m.value = e.weight + a
10:         m.dest = e.dest
11:         write m into the message list of the partition
            whose vertex set contains m.dest in external
            memory
12:      end for
13:   end for
14:   Gather:
15:   for each partition do
16:      read vertex set from external memory and store into
         on-chip memory
17:      for each message m in message list do
18:         read weight of vertex m.dest from on-chip
            memory
19:         let b = weight of vertex m.dest
20:         if m.value < b then
21:            weight of vertex m.dest = m.value
22:            update weight of vertex m.dest in on-chip
               memory
23:         end if
24:      end for
25:      write vertex set into external memory
26:   end for
27: end while
```



Target platform



Memory power optimization



Data layout optimization

Experimental Results

Alg.	Approach	Sustained BW (GB/s)	Throughput (MTEPS)	MTEPS Imprv.	Power (W) DRAM	Power (W) FPGA	Energy-eff. (MTEPS/W)	MTEP/W Imprv.
SSSP	Optimized	15.3	731	3.6×	0.49	23.73	30.2	8.9×
	Baseline	5.3	202		0.51	58.52	3.4	
WCC	Optimized	17.3	862	3.7×	0.49	17.42	48.1	5.8×
	Baseline	6.0	235		0.51	38.13	8.2	
MST	Optimized	16.9	845	3.7×	0.49	18.57	44.3	5.8×
	Baseline	5.9	230		0.51	39.76	7.6	

This work is supported by the U.S. National Science Foundation under grants CCF-1320211 and ACI-1339756.

Email: *{shijiezh, chelmis, prasanna} @ usc.edu*
Web: *ganges.usc.edu*

Ming Hsieh Institute
Ming Hsieh Department of Electrical Engineering