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Pico-Power PLL Charge Pump

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PLL Overview

- *Phase-Locked Loops (PLLs) synthesize high-frequency clocks for radios, processors, and implants*
- PLL output generated by Voltage-Controlled Oscillator (VCO) or Current-Controlled Oscillator (ICO)
- VCO output is compared to a Reference Clock (usually crystal-based)
- Charge Pumps use Phase/Frequency Detector (PFD) error signals to generate VCO control input

Charge Pump Challenges

- Fast and accurate response mandatory to minimize PLL "dead zone" and output errors
- Switching noise near equilibrium point (frequency lock) causes undesired VCO jitter
- State of the art designs traditionally use current mirrors which have these pitfalls:
  - Large area due to many transistors
  - Current always on: high power (i.e. 0.5-1.5mW)
  - High sensitivity to process variation
  - Difficulty switching current sources ON/OFF

Approach

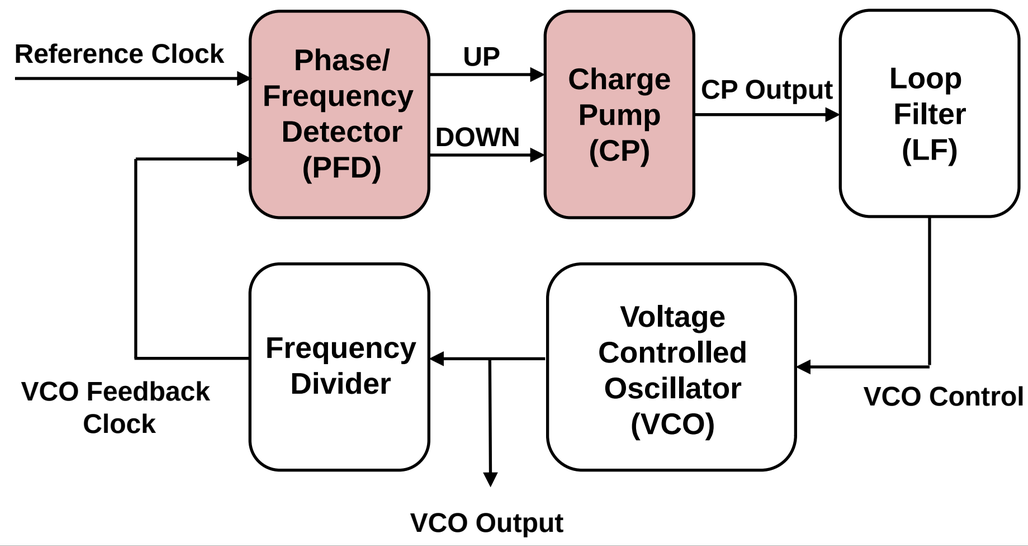
- Eliminate continuous current consumption
  - Replace current source with "flying capacitor"
  - Changes voltage by transferring charge
- Minimize number of active components

PFD/CP Performance Summary

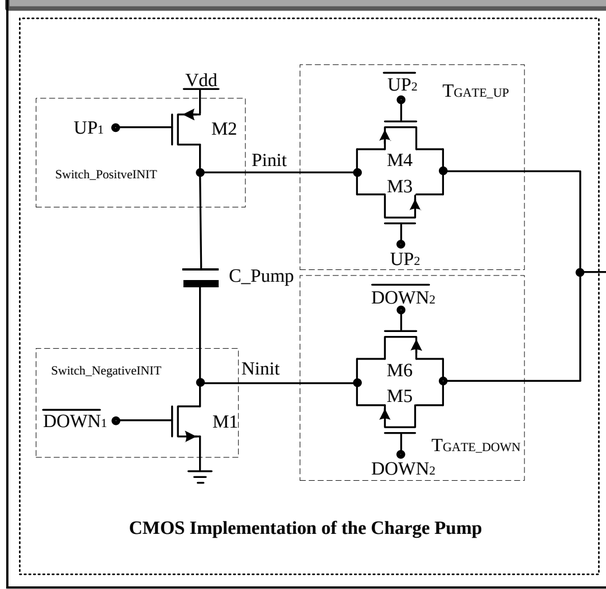
- Ultra Low Power (e.g. 250pW)
  - *10^6 improvement over conventional CPs*
- Insensitive to parametric process variations (e.g. threshold voltage); transistors can also operate in weak to moderate inversion if desired
- Excellent auto-management of VCO control voltage step size:
  - C_Pump and C_LoopFilter capacitor size ratio for large frequency errors
  - Very precise in reaching phase lock
  - Extremely low (<1µV) noise output for small phase errors
- Very compact (30µm x 40µm in 180nm CMOS NSC) – 6 small transistors and a small (e.g. 500fF) capacitor

MODULE	POWER	AREA	COMMENTS
Charge Pump (CP)	253pW	30µm x 40µm	Ultra Low Power/Compact Design; PATENTED
Phase Frequency Detector (PFD)	9.822nW	10µm x 40µm	40ns Dead Zone; PATENTED
Total for PFD/CP	10.075nW	40µm x 40µm	Fabricated in 180nm NSC CMOS; 1.8V supply

PLL System Diagram

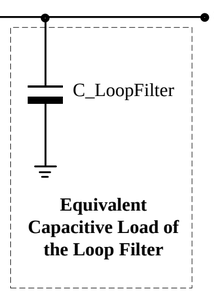


Novel Charge Pump Design



CMOS Implementation of the Charge Pump

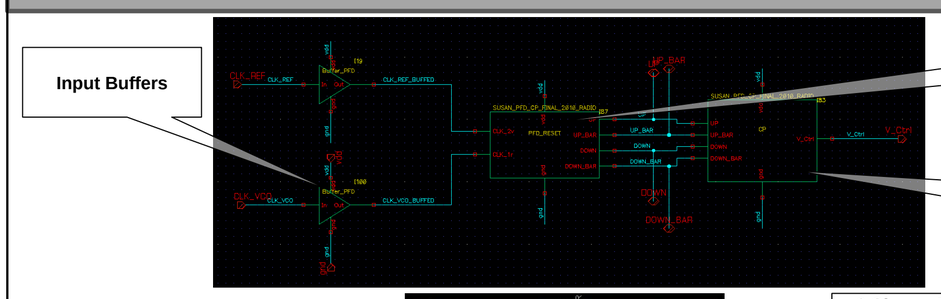
This new approach to PLL Charge Pump design is based on the concept of charge transfer in switched capacitors unlike conventional current based designs.

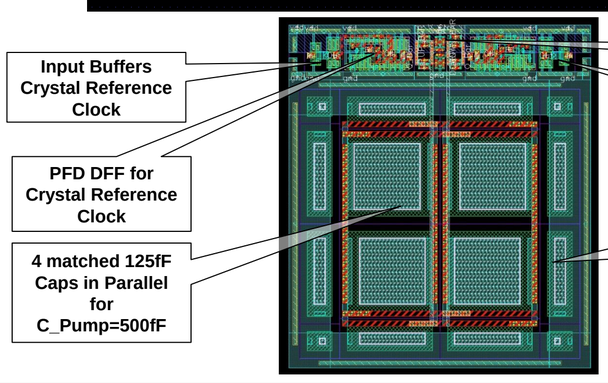


Equivalent Capacitive Load of the Loop Filter

US Provisional Patent # 61/394,908

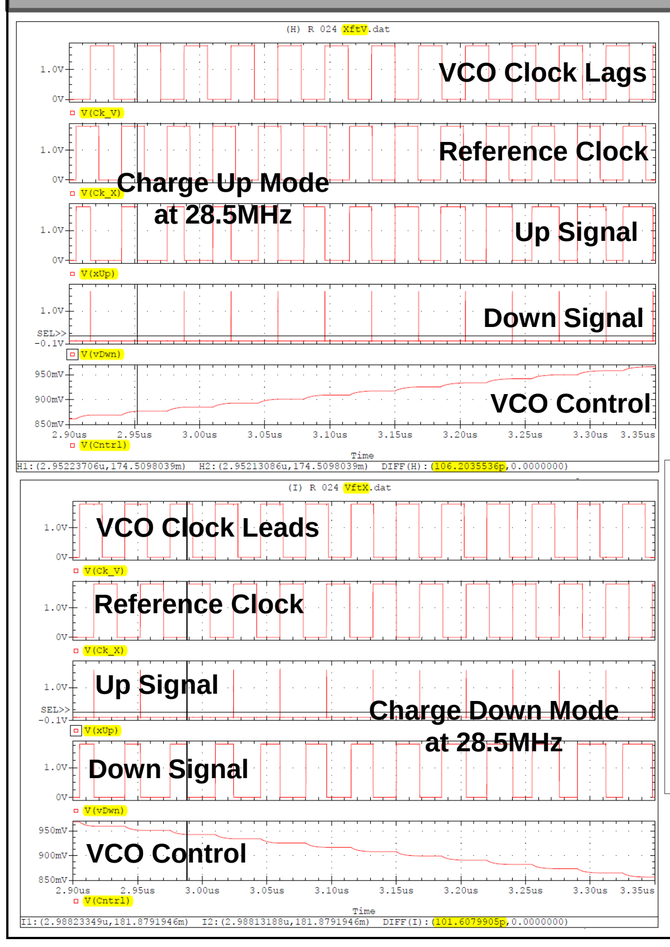
PFD/CP Schematics and Layout

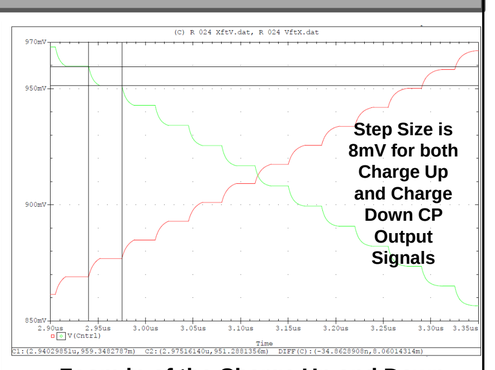




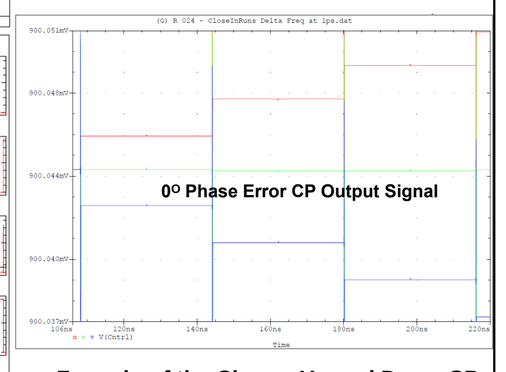
Design Tools Used: Pspice, Matlab, and Cadence

PFD/CP Waveforms





Zoom in of the Charge Up and Down CP outputs at 28.5MHz for a frequency error of 10ns (0.1^O)



Zoom in of the Charge Up and Down CP outputs at 28.5MHz for a phase error of 1ns (0.01^O), and when in phase lock (0^O error shown in Green)

This research is funded by DARPA REMIND, USC BMES ERC, and Texas Instruments/National Semiconductor

Patented with assistance from the USC Stevens Institute for Innovation

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