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Wideband Frequency Synthesis with Rapid Frequency Hopping

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Motivation

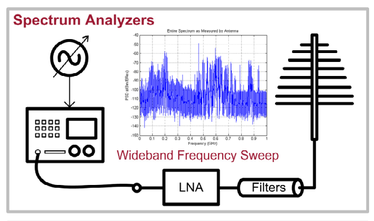
Conventional Spectral Analysis:

- The sweep rate of synthesizer based spectrum analyzers is limited to the acquisition and tracking of phase-locked loops (PLLs).
- Direct digitization and FFT requires high-speed data converters that consume a lot of power.

Key Applications:

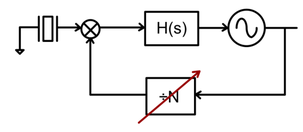
- Spectrum analyzer with small sweep time and real-time power measurement.
- Secure communications over a wideband with rapidly hopping carrier frequency.
- Multi-band OFDM applications in ultra-wideband (UWB) communications.
- Multi-standard wideband downconversion with high modulation bandwidths.

Objective: Design a low power, low noise Rapid-Hopping Frequency Synthesizer with high spectral purity and frequency resolution



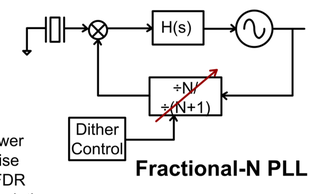
Limits of Standard Techniques

Wideband Frequency Generation Techniques



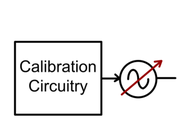
Integer-N Phase-Locked Loop (PLL)

- ✓ Low Power
- ✓ Low Noise
- ✓ High SFDR
- × Low Resolution
- × Very Slow



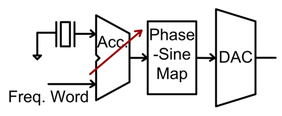
Fractional-N PLL

- ✓ Low Power
- ✓ High Resolution
- ✓ Low Noise
- × High Fractional Spurs
- × Slow



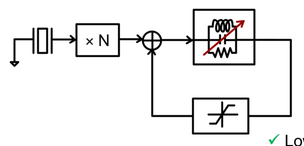
Free-Running Oscillator

- ✓ Low Power
- ✓ High Resolution
- ✓ Very Fast
- × Very High Noise



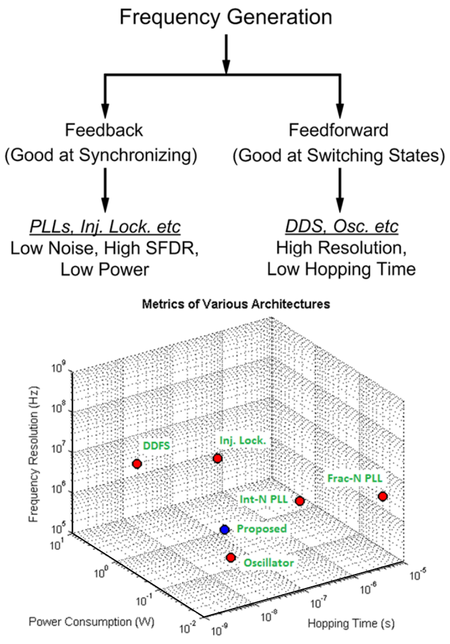
Direct Digital Frequency Synthesis (DDFS)

- ✓ High Resolution
- ✓ Fast
- × High Power
- × Low SFDR

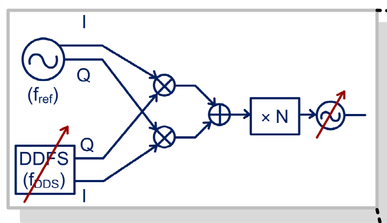


Frequency Multiplication and Locking

- ✓ Low Power
- ✓ Very High Noise
- ✓ Very Fast
- × Low Resolution
- × Low SFDR

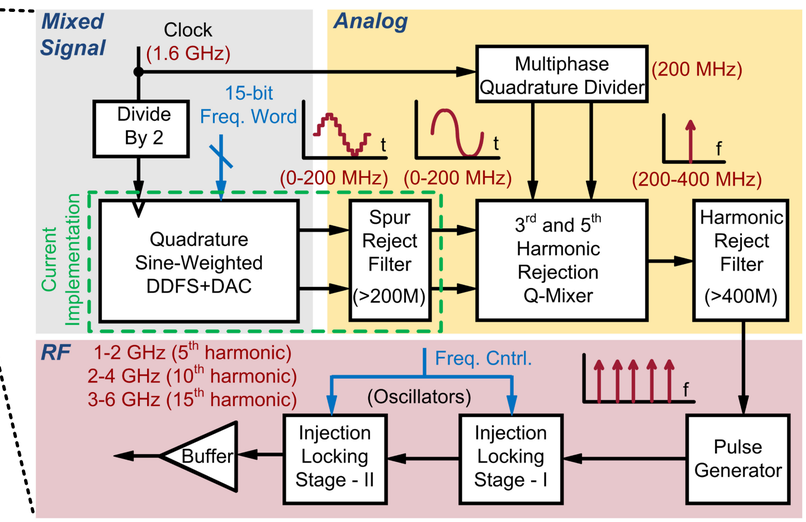


Proposed Architecture



Highlights of Architecture:

- Wideband frequency generation by the method of multiplication (covers 1-6 GHz).
- High resolution using a 15-bit frequency word (24 KHz at baseband and 366 KHz at RF).
- Rapid hopping using a sine-weighted DDFS that has no state machines and hence low latency.
- Bandpass response of injection locking stage reduces spurs and increases out-of-band SFDR.
- High frequencies are generated using injection locking of harmonics of baseband tones, thus making overall system low-power.



Signal Path

DDFS	Filter	Upconvert	Filter	Harmonics	Locking	System	
Sine-Weighted DDFS	6-Stage Chebychev BiQuad	Harmonic Reject Q-Mixer	6-Stage Chebychev BiQuad	Fast Latch with Pulse Narrowing	Quadrature Ring/LC Oscillator	**1-6 GHz Frequency Synthesizer**	Design Choice
10 ns	15 ns	-	15 ns	-	4 ns	44 ns	Hopping Time
55 dB	65 dB	50 dB	65 dB	-	60 dB	45 dB	SFDR
173 mW	63 mW	25 mW	48 mW	1 mW	20 mW	450 mW	Power

General Working Principle

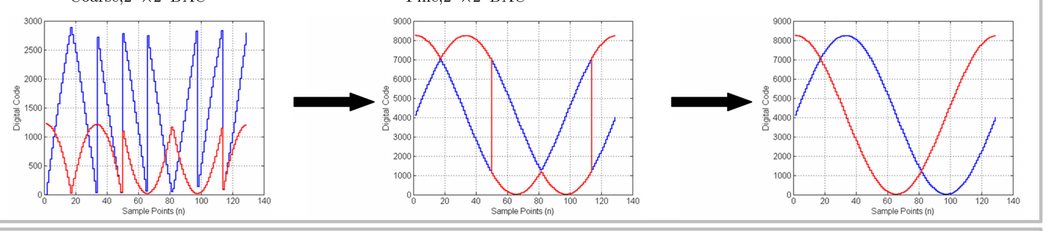
Baseband (0-200 MHz)

Phase Segmentation and DAC Output (after Quarter-wave Compression):

$$V_{out} \approx \underbrace{A\sin\left(2\pi\frac{x\cdot 2^{b+c}+y\cdot 2^{c}}{2^{P-3}}\right)}_{\text{Coarse, } 2^4\times 2^4\text{DAC}} + \underbrace{A\cos\left(2\pi\frac{x\cdot 2^{b+c}+\bar{y}\cdot 2^{c}}{2^{P-3}}\right)\sin\left(\frac{2\pi z}{2^{P}}\right)}_{\text{Fine, } 2^4\times 2^4\text{DAC}}$$

$$a+b+c=P-3;\ A=2^{M}-1$$

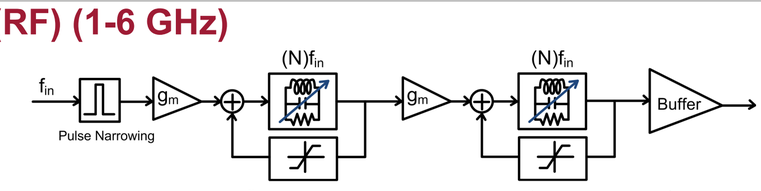
P = Frequency Word Length
M = DAC Resolution



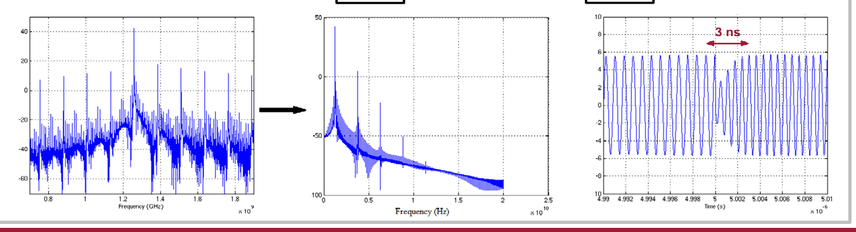
Radio Frequency (RF) (1-6 GHz)

Phase Dynamics:

$$\underbrace{\tan(\alpha/2)}_{\text{Phase Error}} \propto -\tanh\left(\underbrace{\frac{\epsilon N f_{in}}{2Q\Delta f}t}_{\text{Loop Gain}}\right)$$

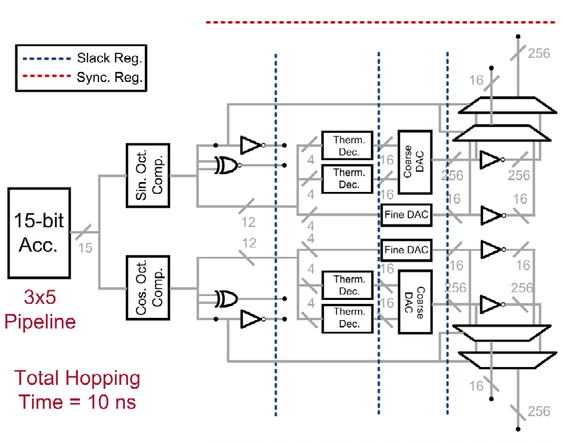


- Q = Quality Factor
  ε = Injection Gain
  Δf = Initial Frequency Offset
- Hopping Time proportional to $1/Nf_{in}$



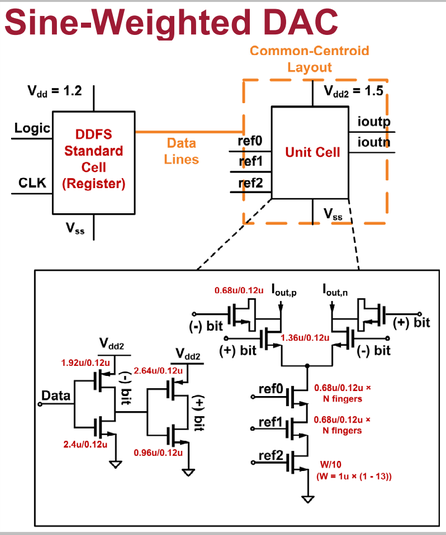
Integrated Circuit Implementation

DDFS



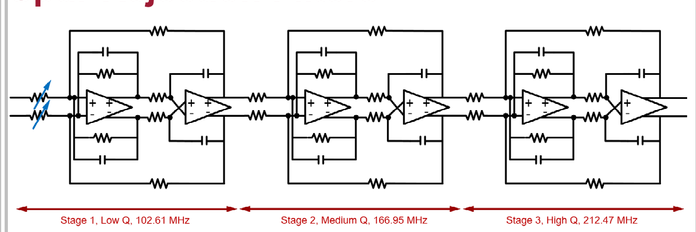
- DDFS is a 15-bit accumulator with phase compression, phase segmentation and binary-to-thermometer converters.
- Theoretical SFDR of DDFS is 58 dB, due to the sine-weighted approximations.
- Synthesis and timing analysis performed using Synopsys® and automatic place-and-route layout with extraction performed using Cadence SOC Encounter®.
- Total hopping time of 10 ns due to registers included to meet slack requirements.

Sine-Weighted DAC



- Phase compression results in a DAC resolution of 13 bits.
- Besides coarse and fine DACs, MSB DACs are used to perform amplitude decompression.
- Final waveforms are swapped using swapping switches to generate quadrature waveforms.
- Sizes of current sources are large to reduce overall mismatch.
- Current sources are laid out in a pseudo common centroid manner to minimize systematic layout-related error.

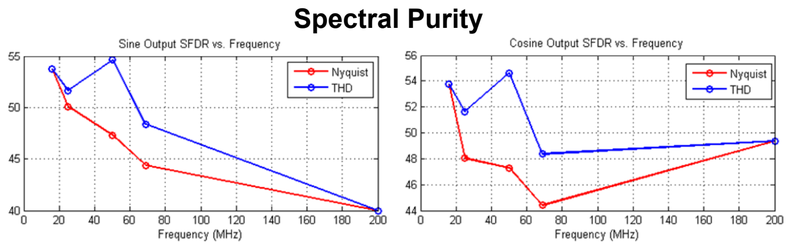
Spur Rejection Filters



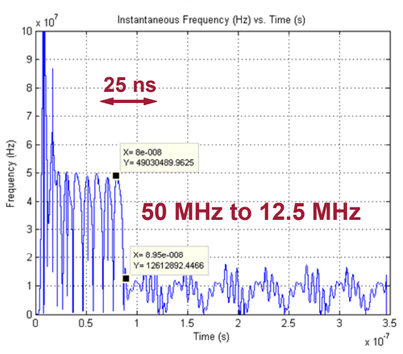
- Filter of passband 200 MHz and > 60 dB rejection at 600 MHz is required to reduce spurs to below the harmonics.
- Design choice is 6th-order Chebychev filter implemented as a 3-stage OTA-RC biquad structure that achieves > 65 dB SFDR.
- Hopping time of the filter system is atmost 15 ns between any two frequency hops.

Schematic Simulations

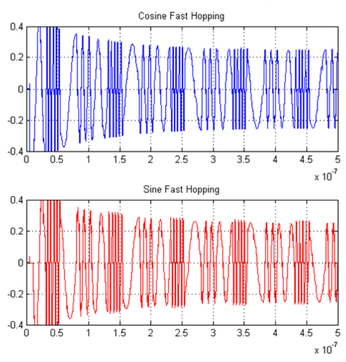
Spectral Purity



Single Hop



Rapid Hopping

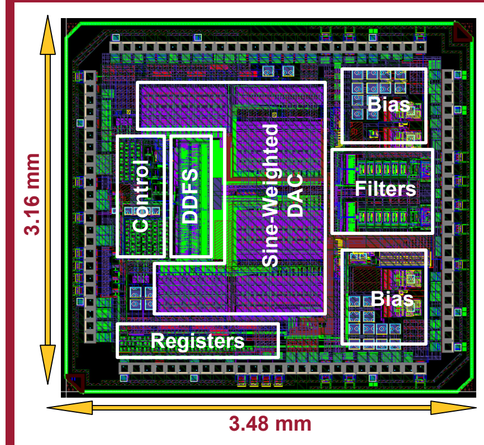


Performance Results

(Results Specified for Baseband)

Specification	Achieved Result
Process	0.13 µm CMOS
Reference Clock	800 MHz
Frequency Range	0-200 MHz
Frequency Resolution	24.41 KHz
DAC Resolution	13 bits
Phase Noise	-120 dB/Hz (at 1 MHz offset)
Frequency Stability	(reference dependent)
SFDR	45 dB (66 MHz) 40 dB (200 MHz, before filters)
Hopping Time	25 ns
Power Consumption	V_{dd} = 1.2 V, 150 mW V_{dd} = 1.5 V, 238 mW
Chip Area	11.02 mm^2 (including pads)

Chip Layout and Conclusions



- A 1-6 GHz synthesizer optimized for SFDR, Hopping Time, Power Consumption and Frequency Resolution
- Phase 1 (Baseband) complete
  Phase 2 (RF) under design

Future Work

- Preparation of Chip Package and Testing Board.
- Measurement and Characterization of Baseband (DDFS + Filter) Chip.
- Design of complete system and possible use in existing software defined radio (SDR) applications.
- Enabling high-bandwidth modulation and secure transceivers using custom, fast digital control circuits.
- Circuit Sychronization consists of two aspects: Acquisition and Tracking; can concepts of fast-acquisition in fast hopping synthesizers be used in fast-tracking applications?

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