Ming Hsieh Department of Electrical Engineering

Tunable Algorithms for High Energy Efficiency

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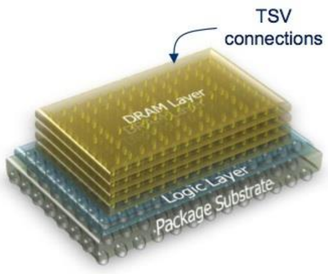
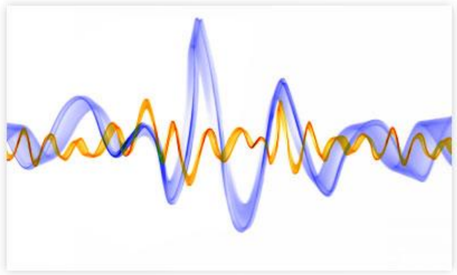
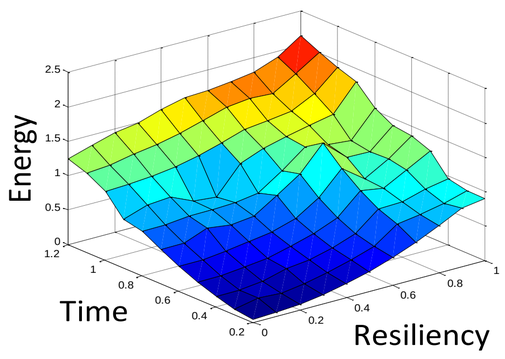
Motivation





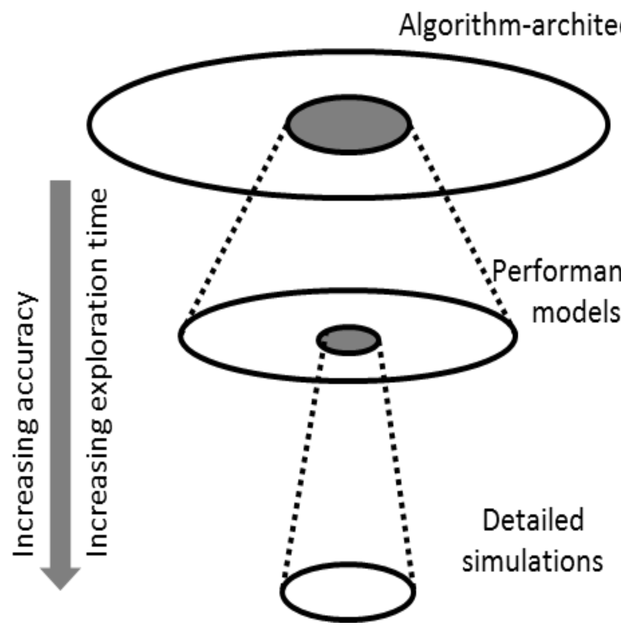


Functioning prototypes in silicon TODAY

Architecture | Application | Energy

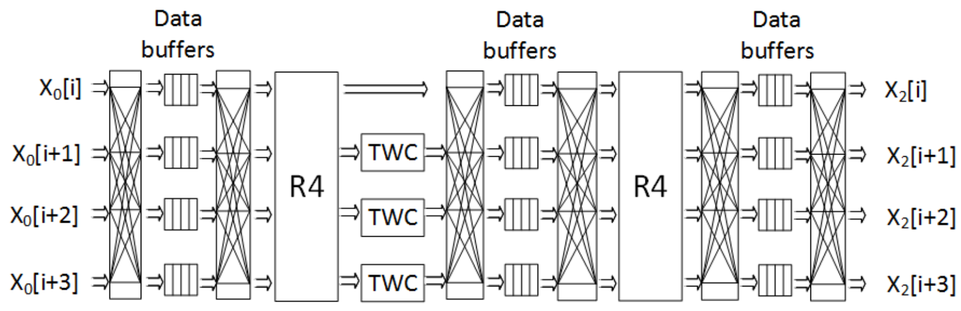
Tunable Algorithms for Energy Efficiency using Emerging Architectures

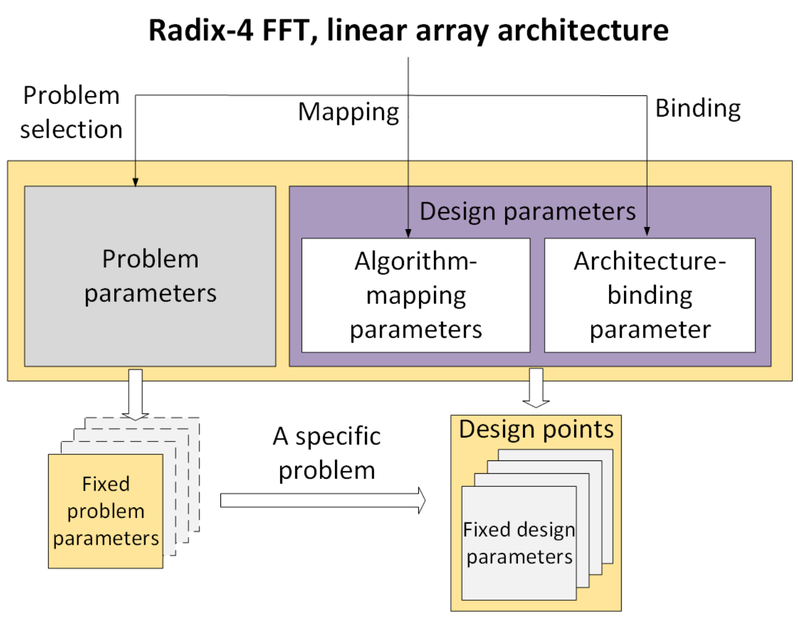
Introduction



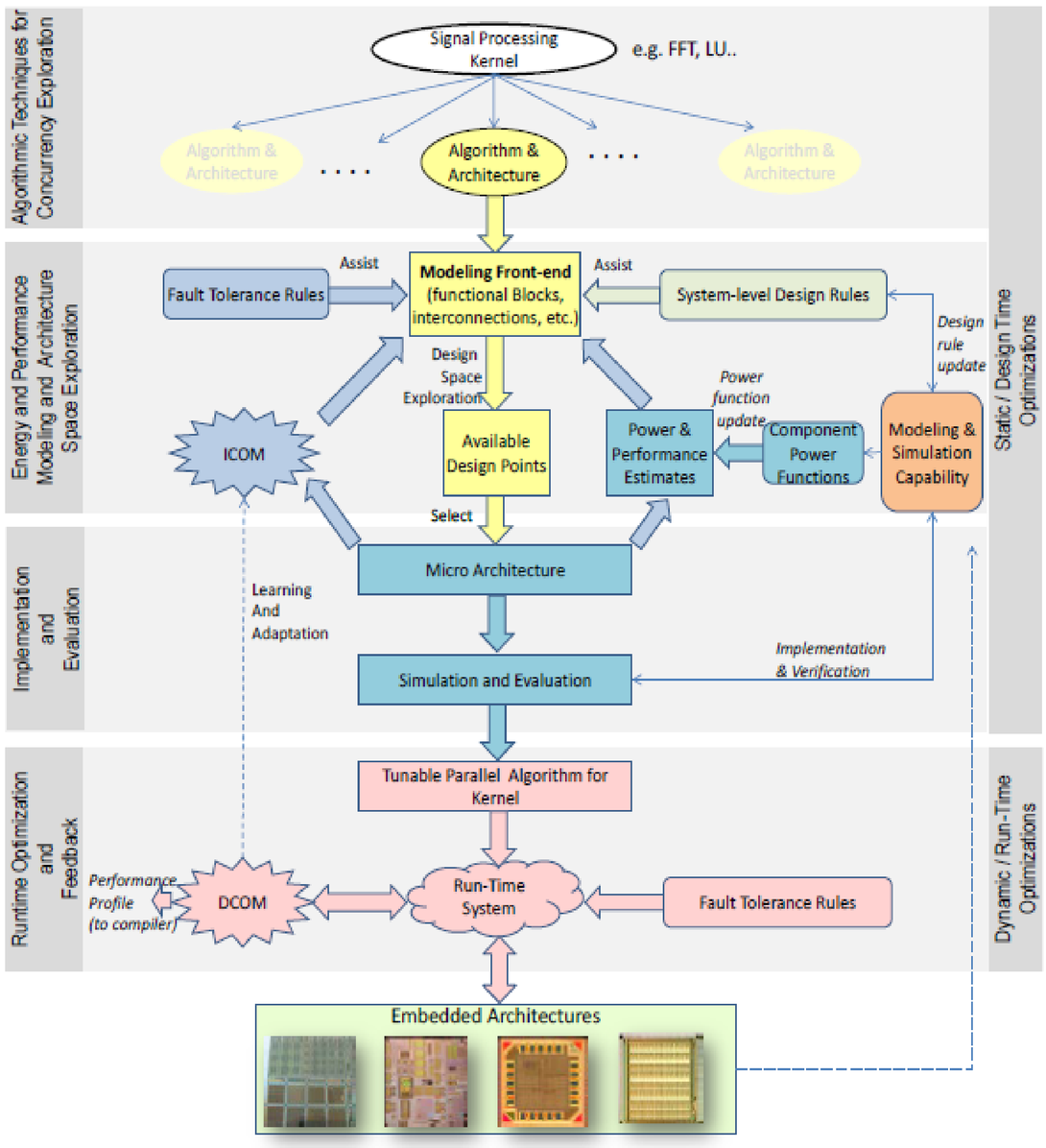
Tunable Algorithms for 1-D FFT

Problem parameters	Design parameters	
Problem size Data width Data precision	Vertical parallelism Horizontal parallelism	Type of memory Type of interconnection Pipeline depth

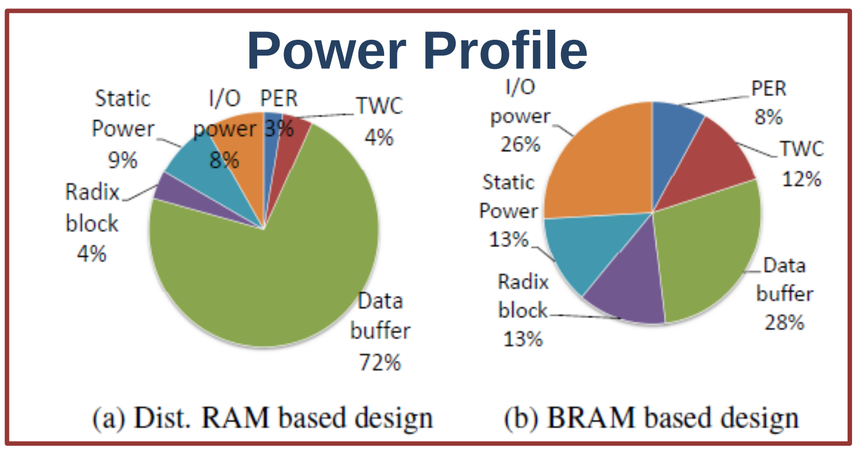




Design Methodology



Algorithm Techniques



Time-multiplexing

Periodic memory activation

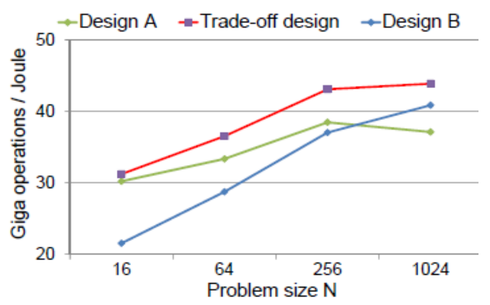
Design Space Exploration

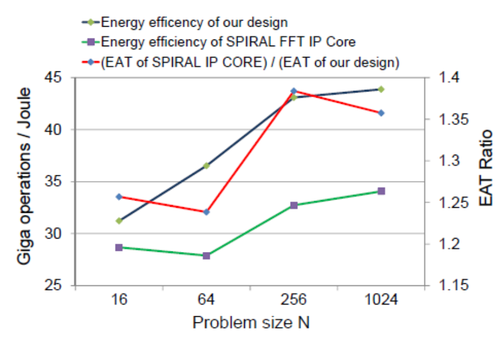
Design space

- Estimated energy performance
- Determined design points
- Identified superior designs

Performance comparison

- SPIRAL IP Cores
  - Radix-4
  - Natural-in and natural-out data
  - 16-bit fixed point, fully streaming
- Performance improvement
  - 8%-28% in energy efficiency
  - 8%-38% in EAT
- Sustained energy efficiency
  - 78% of the Peak Energy Efficiency





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