

Motivation

Functioning prototypes in silicon TODAY

Architecture Application Energy

Tunable Algorithms for Energy Efficiency using Emerging Architectures

Introduction

Algorithm-architecture pairs

Performance models

Detailed simulations

Increasing accuracy

Increasing exploration time

Tunable Algorithms for 1-D FFT

Problem parameters	Design parameters	
Problem size Data width Data precision	Vertical parallelism Horizontal parallelism	Type of memory Type of interconnection Pipeline depth

Radix-4 FFT, linear array architecture

Problem selection Mapping Binding

Problem parameters Design parameters

Algorithm-mapping parameters Architecture-binding parameter

Fixed problem parameters A specific problem Design points

Fixed design parameters

Design Methodology

Algorithmic Techniques for Concurrency Exploration

Energy and Performance Modeling and Architecture Space Exploration

Implementation and Evaluation

Runtime Optimization and Feedback

Static / Design Time Optimizations

Dynamic / Run-Time Optimizations

Signal Processing Kernel (e.g. FFT, LU...)

Algorithm & Architecture

Modeling Front-end (functional blocks, interconnections, etc.)

Available Design Points

Micro Architecture

Simulation and Evaluation

Tunable Parallel Algorithm for Kernel

Run-Time System

Embedded Architectures

Algorithm Techniques

Power Profile

(a) Dist. RAM based design

(b) BRAM based design

Time-multiplexing

Periodic memory activation

Design Space Exploration

Design space

- Estimated energy performance
- Determined design points
- Identified superior designs

Performance comparison

- SPIRAL IP Cores
 - Radix-4
 - Natural-in and natural-out data
 - 16-bit fixed point, fully streaming
- Performance improvement
 - 8%-28% in energy efficiency
 - 8%-38% in EAT
- Sustained energy efficiency
 - 78% of the Peak Energy Efficiency

Giga operations / Joule

Problem size N

EAT Ratio