A VARIATION AWARE RESILIENT FRAMEWORK FOR POST-SILICON DELAY VALIDATION OF HIGH PERFORMANCE CIRCUITS

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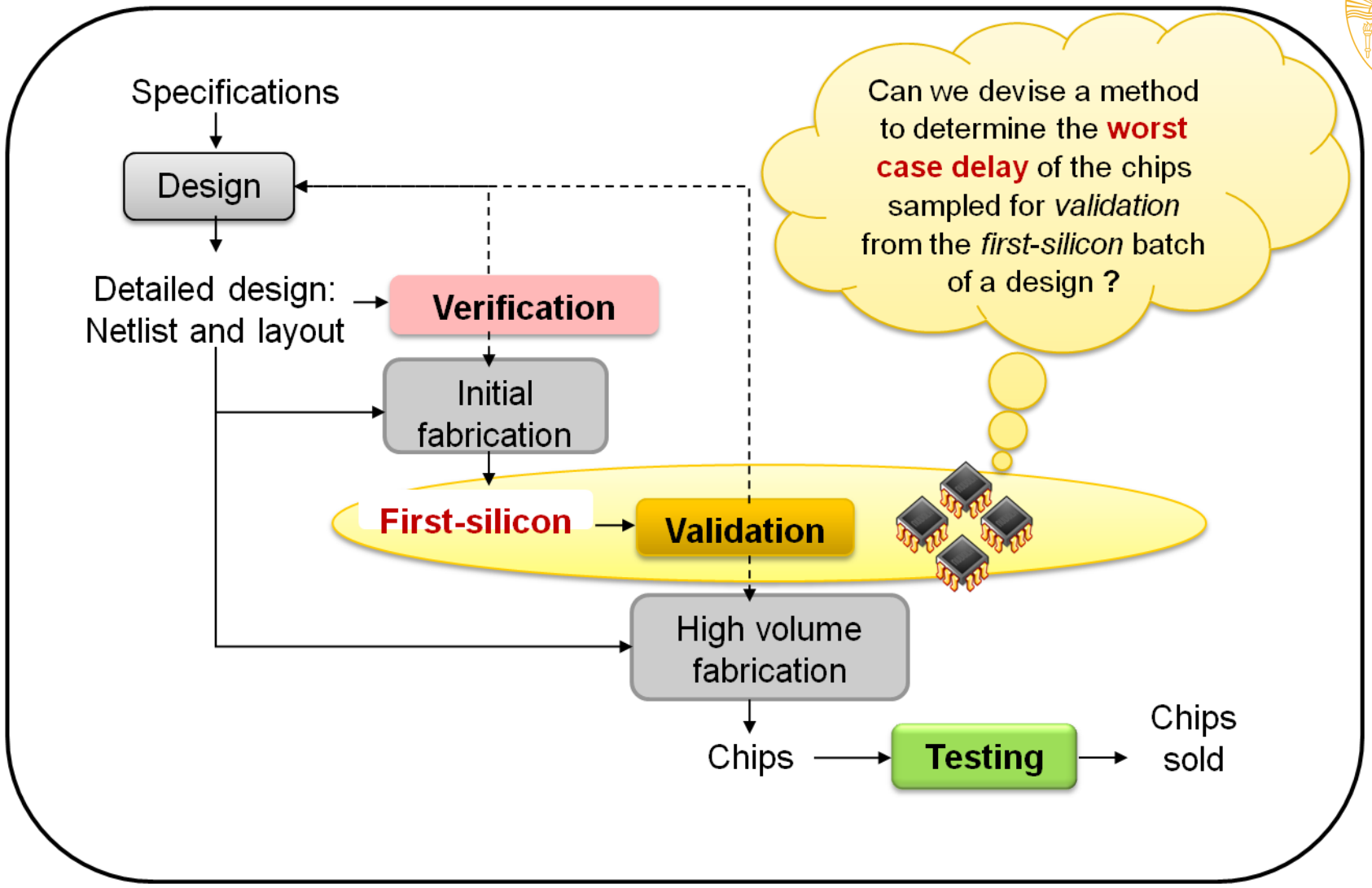
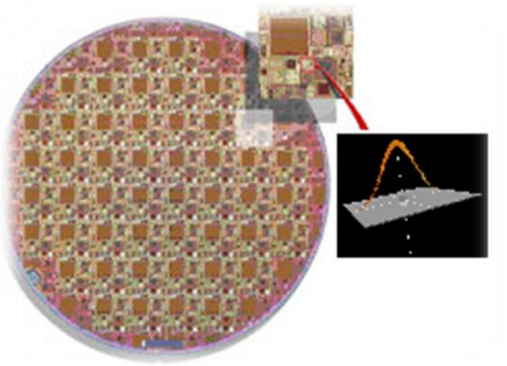

Specifications
Design
Detailed design:
Netlist and layout
Verification
Initial fabrication
First-silicon
Validation
High volume fabrication
Chips
Testing
Chips sold
Can we devise a method to determine the worst case delay of the chips sampled for validation from the first-silicon batch of a design ?

Purpose

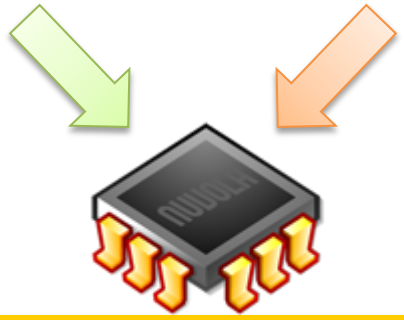
Delay measured on fabricated chips tend to deviate from estimated nominal delay due to

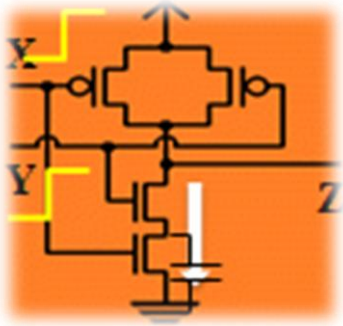
- **Multiple input switching (MIS)**
  - *Increase/decrease* of delay due to lower order effects.
- **Normal process variations**
  - Delay marginalities due to lack of precise fabrication control.

Within scope
hard to detect



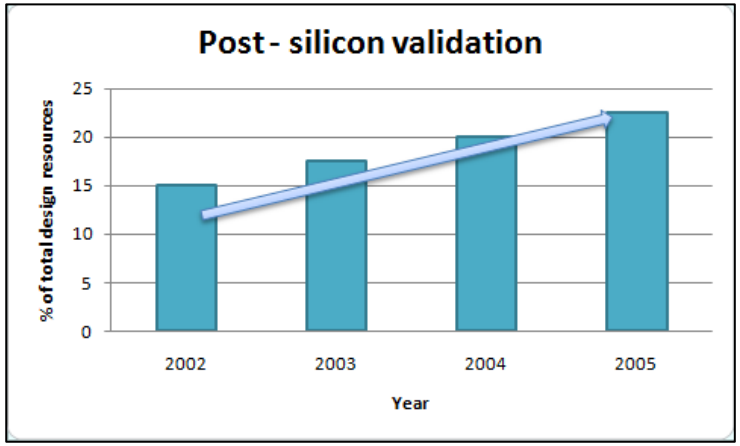
Process variations



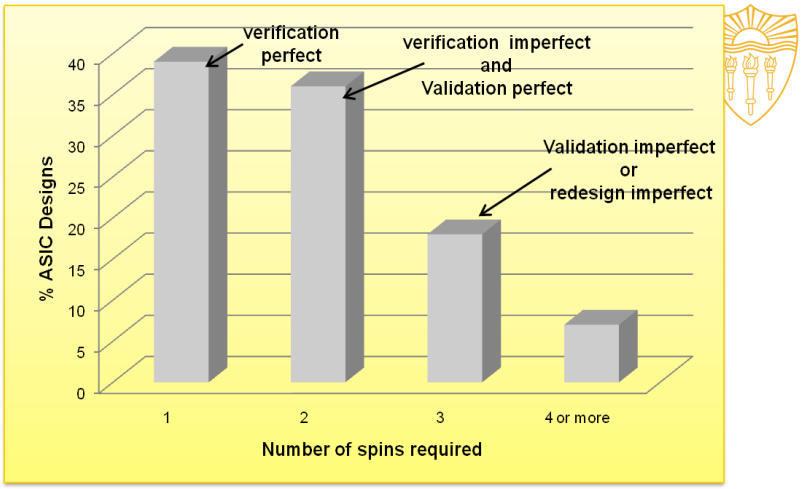


MIS

The scope



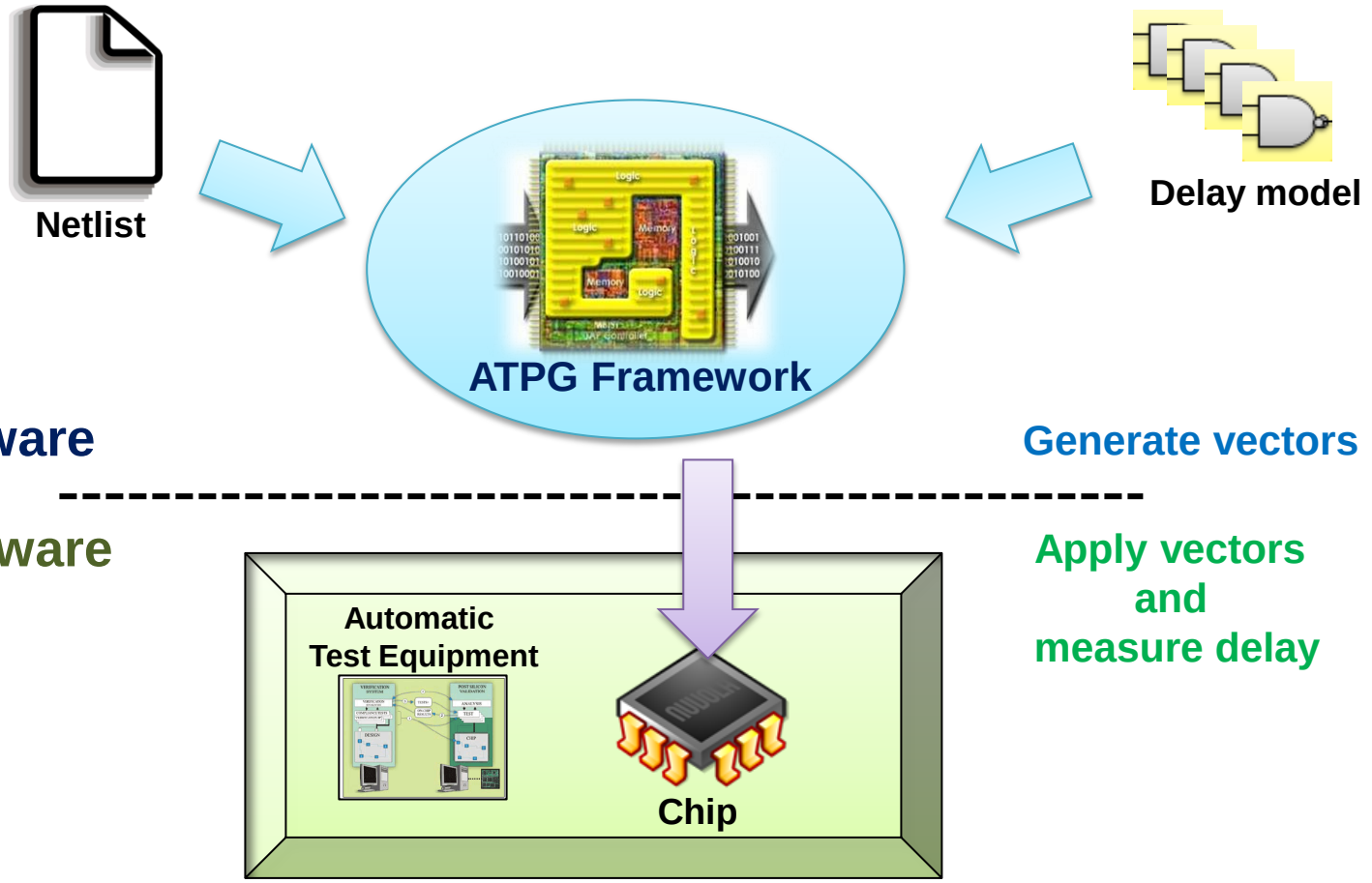
Increasing importance of validation



Current validation approaches inadequate

Current delay-testing approaches inadequate

Motivation

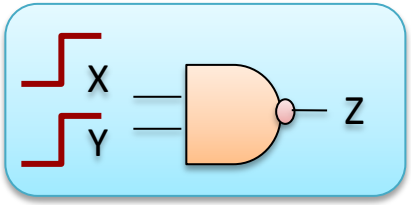


Proposed flow

Bounding approximations to capture variations and MIS using bounds at low complexities.

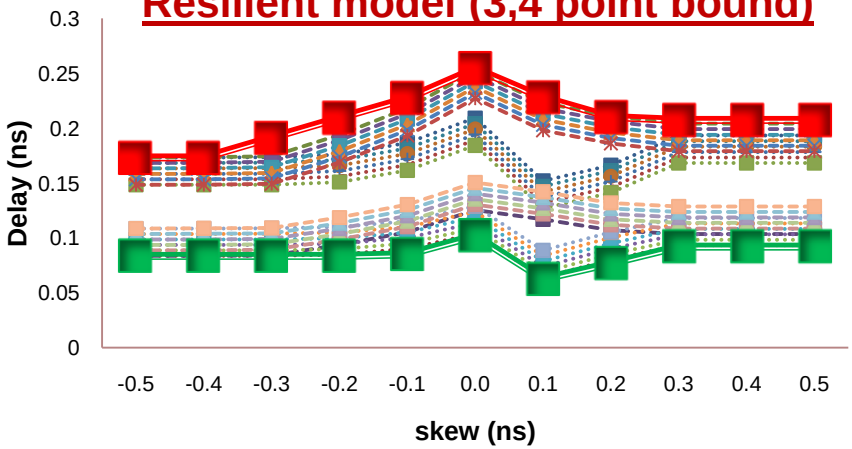
This model captures

- ✓ Input slew
- ✓ Input position
- ✓ Output load.
- ✓ Input skew (MIS)
- ✓ State of internal capacitances
- ✓ Process variations

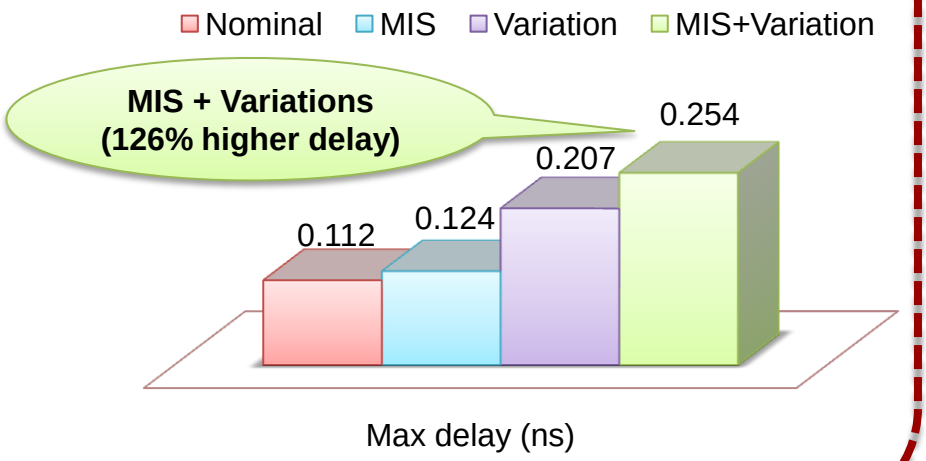


Tight bounds (<5% error)

Resilient model (3,4 point bound)

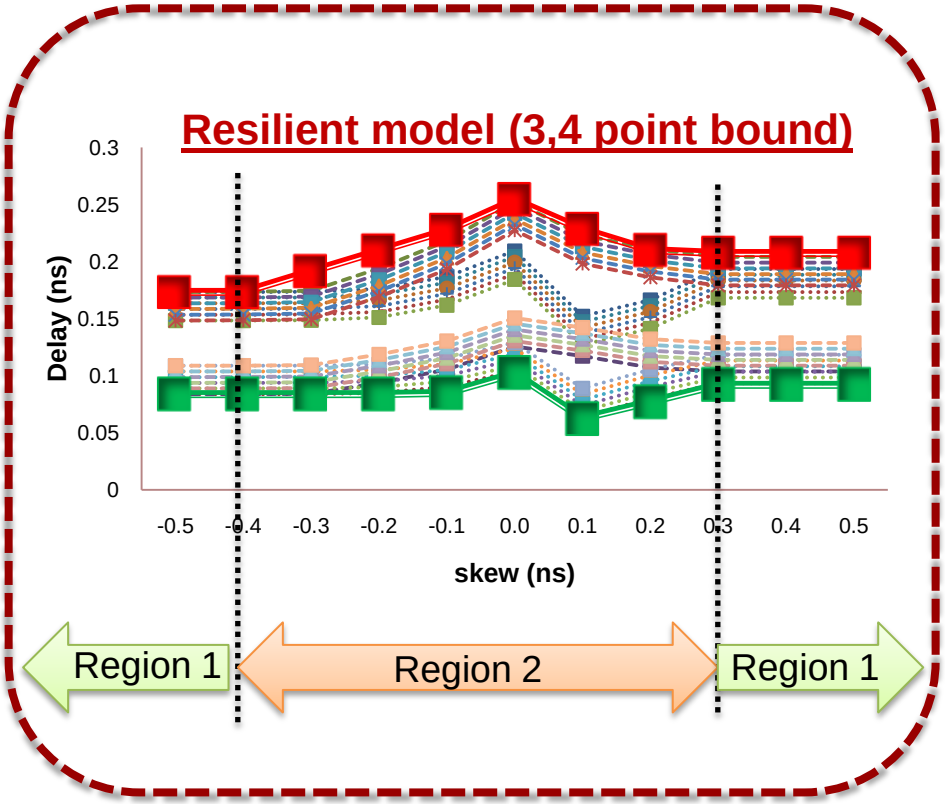


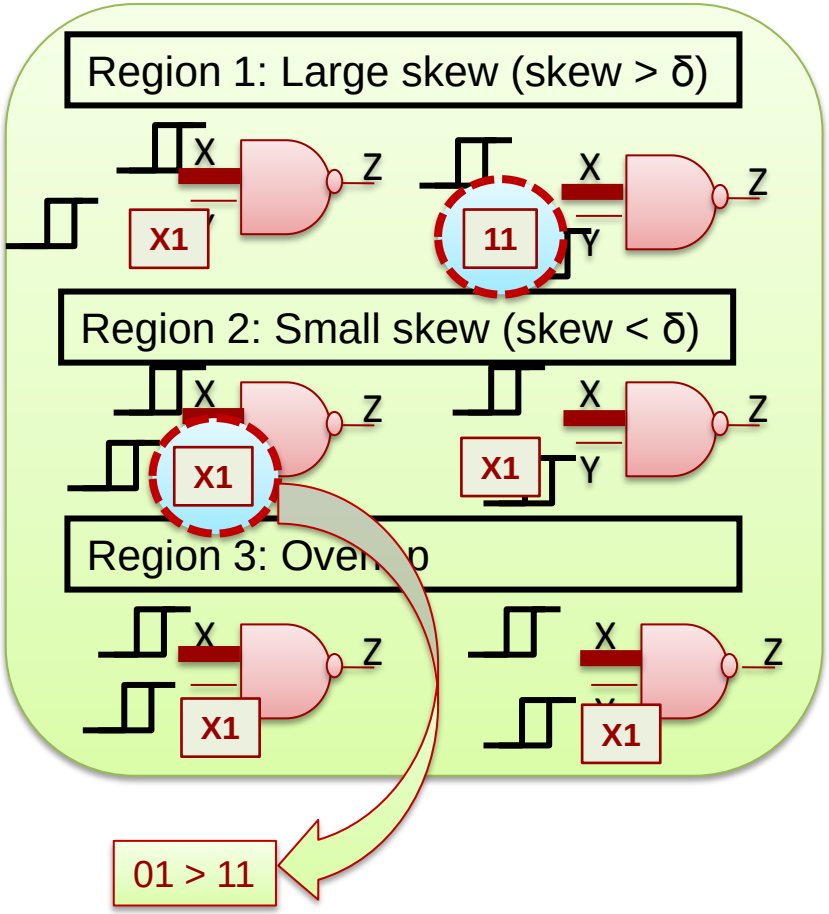
Max delay of a 2-input NAND gate



Resilient delay model

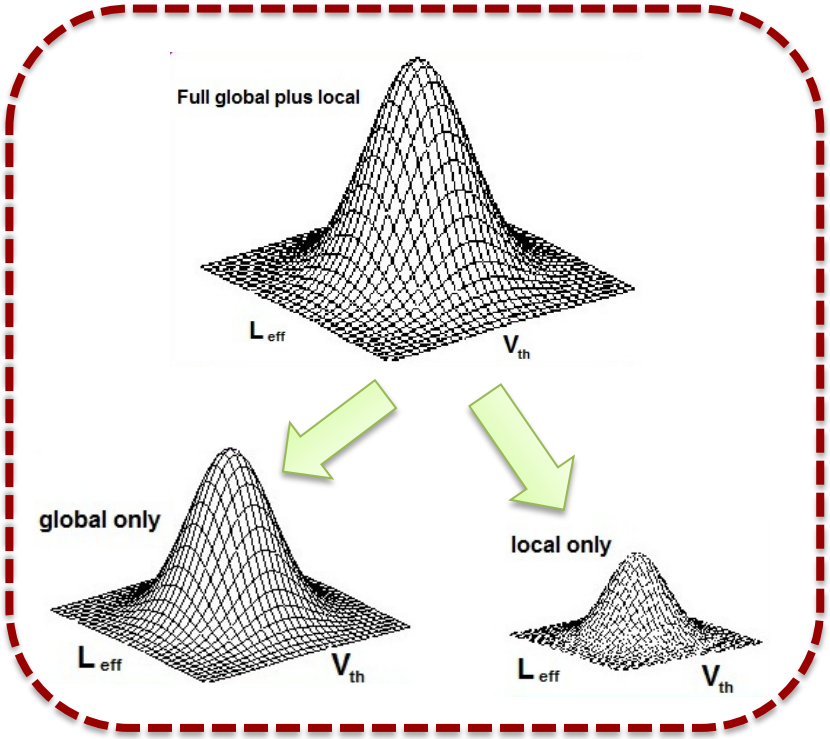
Generate vectors that can account for delay increase due to MIS and process variations

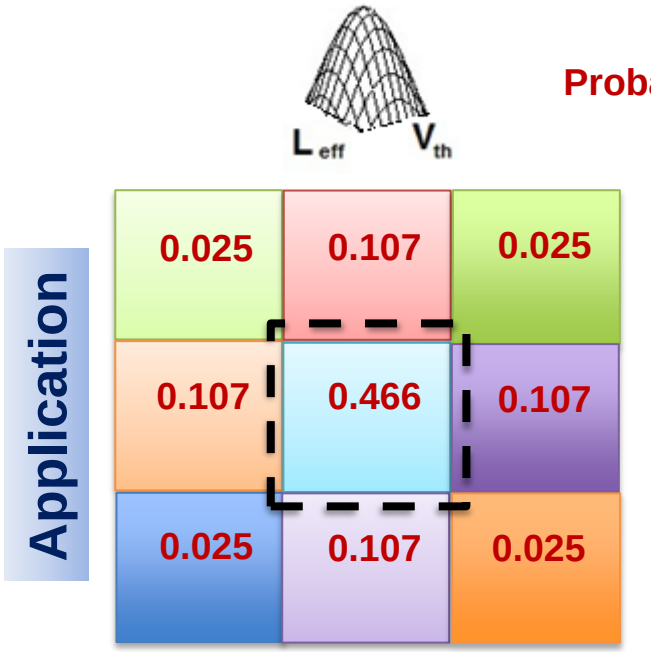




MIS-aware vector generator

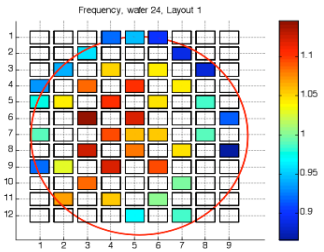
Segment global process variation envelope to reduce test-volume and test application time





Divide and conquer

Global-only process shift can be estimated using ring-oscillator based process monitors.



Variation-aware vector generator

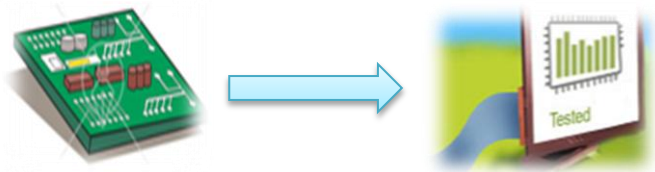
Systematic framework for post-silicon marginality validation

Experiments on real-chip based benchmark
- ❖**5X** reduction in path-set
- ❖**2X** reduction in test-generation time
- ❖**20X** reduction in test-application time
- ❖**10%** higher delay invocation

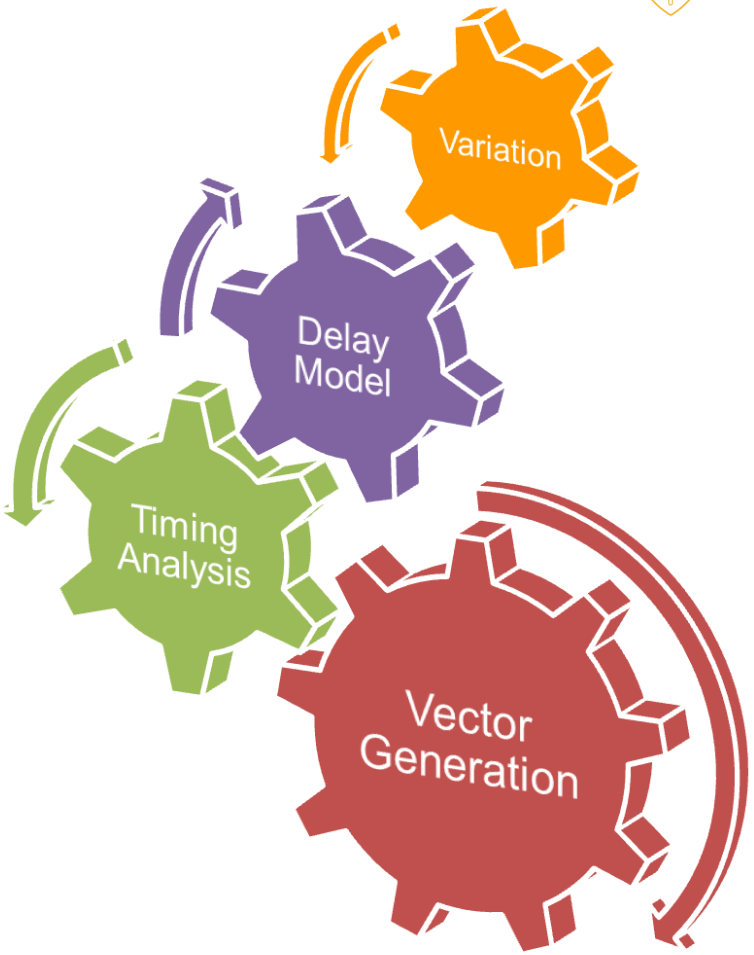
SCAN based post-silicon marginality validation

Silicon experiments on a processor netlist:
- ❖Reduction in path-set
- ❖Tests exposed unique detects
- ❖Tests ran at lower frequency

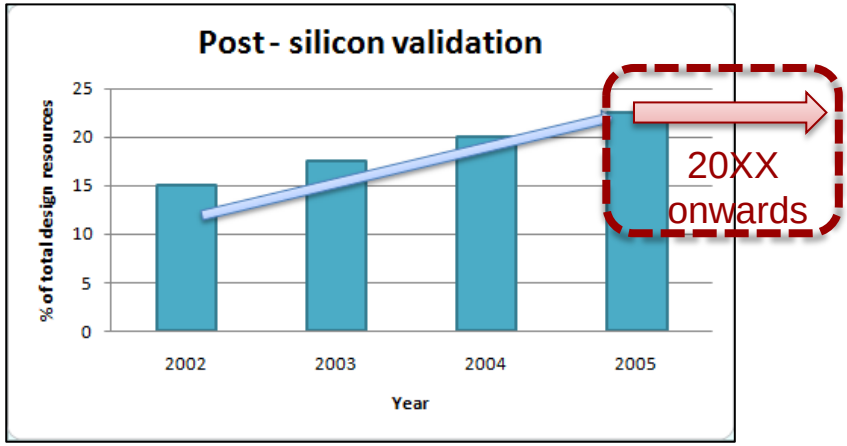
"TEST" learns from "DESIGN"



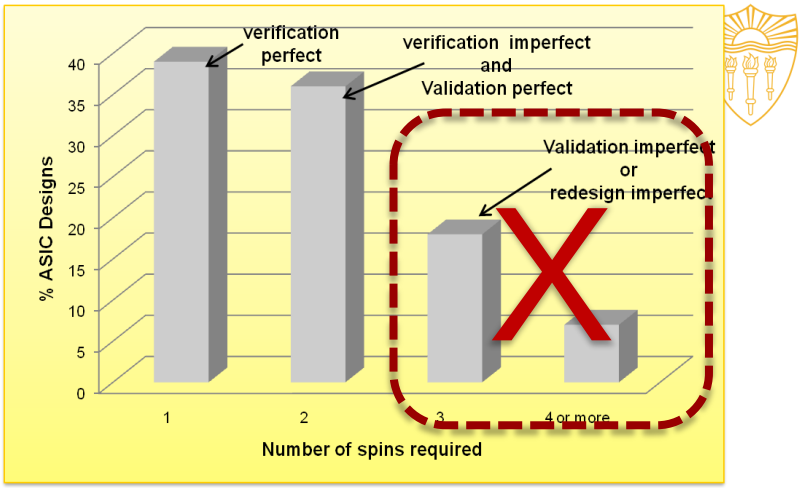
Variation and MIS aware delay validation framework



Short term benefits



~~Increasing~~ importance of validation



~~Current~~ validation approaches ~~inadequate~~

~~Current~~ delay-testing approaches ~~inadequate~~

Long term benefits