Ming Hsieh Department of Electrical Engineering

USC Viterbi School of Engineering

High Performance IPv6 Forwarding on Software and Hardware Platforms

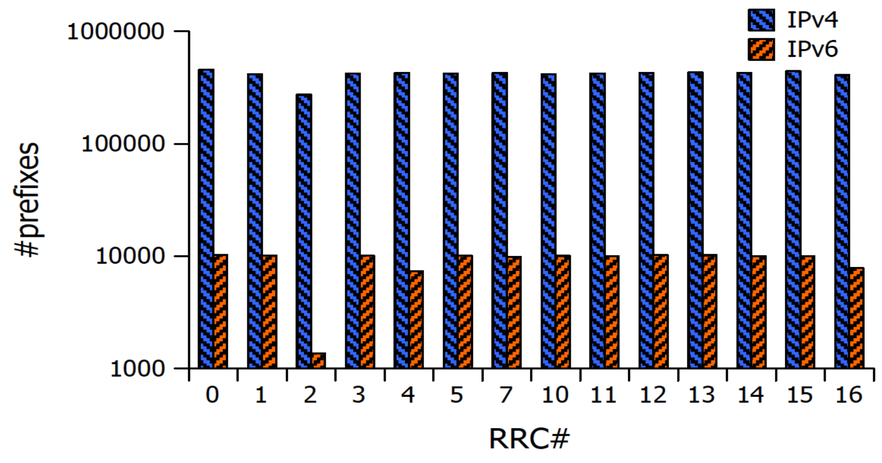
Thilan Ganegedara and Viktor Prasanna
Department of Computer Engineering (Parallel Computing Group)

IPv6 and Backbone Networks

Internet addressing: IPv4 (32 bit) and IPv6 (128 bit)
IPv6 representation in backbone routing tables
- Currently ~2%, but growing

Challenges with IPv6
- Increased packet lookup complexity
- Increased routing table storage requirements

Challenges with Backbone networks require,
- High-speed forwarding (100+ Gbps rates)
- Low-latency operation
- Scalability



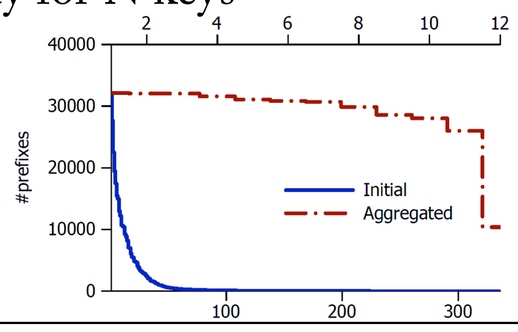
Prefix distribution of current backbone routing tables. With more ISPs adopting IPv6, the IPv6 representation is expected to grow significantly in future

Approach

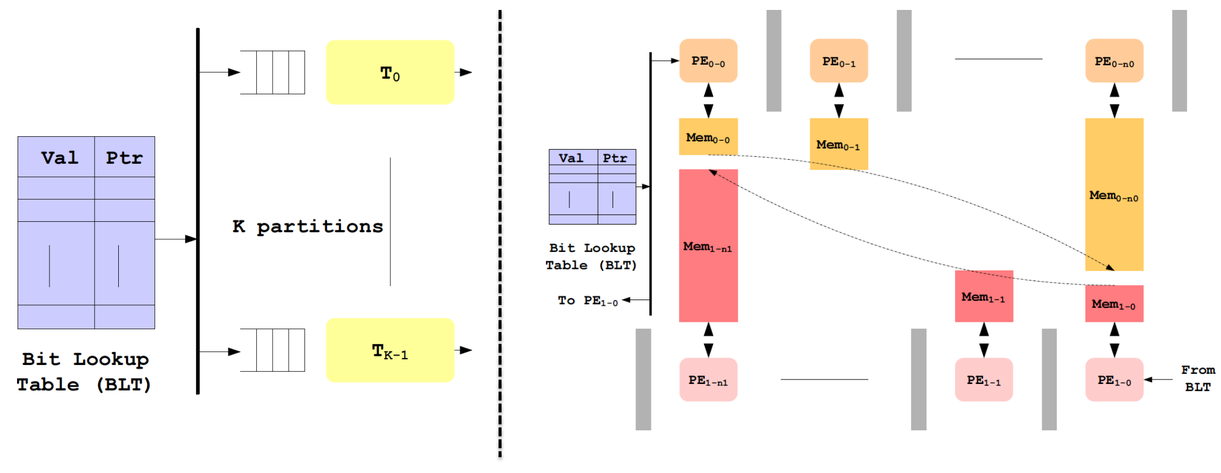
Partition the routing table into disjoint sets – 2 phases
- Phase 1: Use initial *p* bits of prefixes and partition
- Phase 2: Aggregate initial partitions → Near uni-size

Represent each aggregated partition as ***Range tree***
- O(log N) search complexity for N keys
- Higher scalability

Results for a 350K entry backbone routing table (p = 15, n_i = 336, n_a = 12)



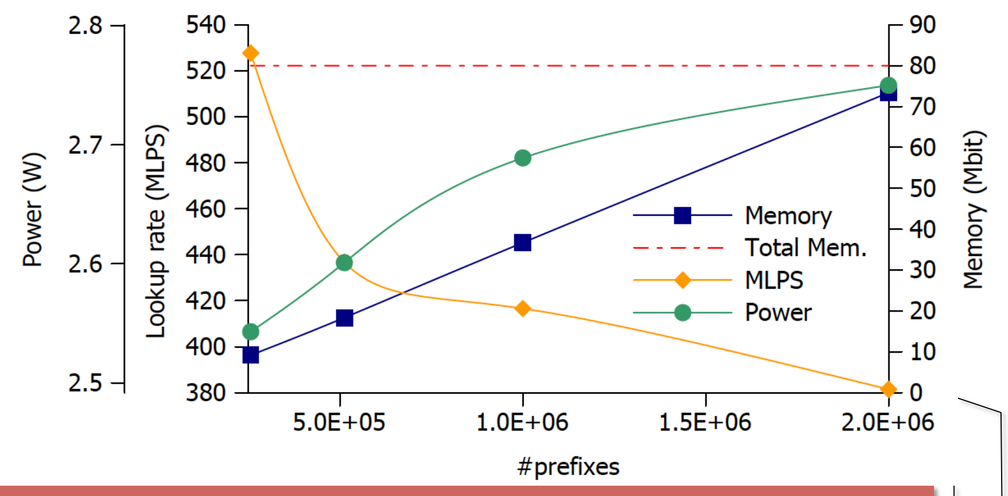
Architectures



Software (multi-threaded) and hardware (multi-pipelined) architectures for the proposed forwarding engine

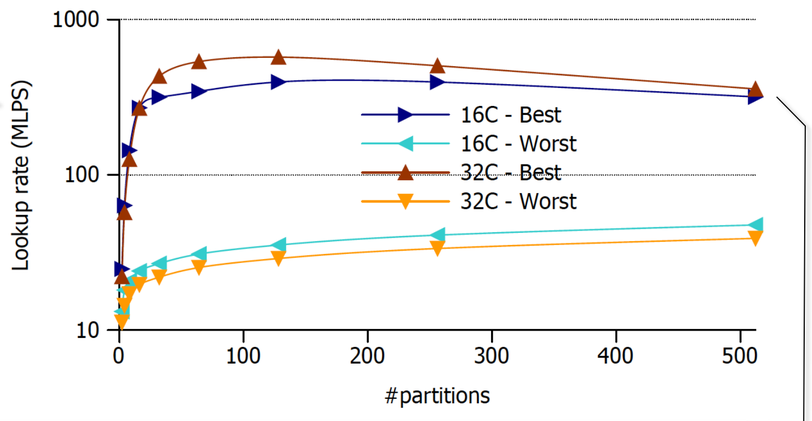
Performance

Routing tables: Large (up to 8M) synthetic routing tables
Platforms:
- AMD Opteron 6278, 32-core @ 2.4 GHz
- AMD Opteron 6220, 16-core @ 3.0 GHz
- Xilinx Virtex 7 X1140T– 80 Mbit on-chip RAM



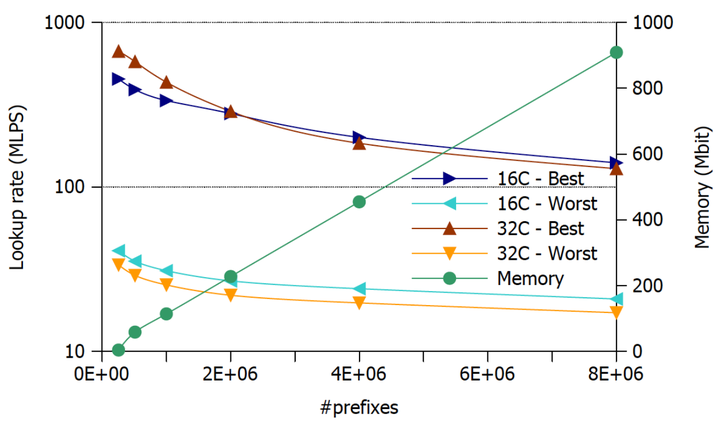
- Able to support 100+ Gbps rates
- Lower power consumption ← Disjoin partitions
- Higher scalability ← Lower memory footprint

Results for varying number of partitions for a 350K entry routing table



Performance tapers off due to increased context switching for increasing number of partitions

Scalability of the software architecture for increasing routing table sizes



Conclusion

- A versatile solution for software and hardware platforms for high performance IPv6 forwarding
- Suitable for 100+ Gbps line-card solutions
- Higher scalability and lower latency with range-tree search
- Lower power consumption on hardware platforms due to disjoint partitioning

Contact: Thilan Ganegedara – ganegeda@usc.edu, Viktor Prasanna – prasanna@usc.edu
This work is supported by the United States National Science Foundation under grant No. CCF-1116781. Equipment grant from Xilinx Inc. is gratefully acknowledged.

Ming Hsieh Institute
Ming Hsieh Department of Electrical Engineering