Ming Hsieh Department of Electrical Engineering

100-Channel Event-Driven Neural Recoding System with Wireless Telemetry

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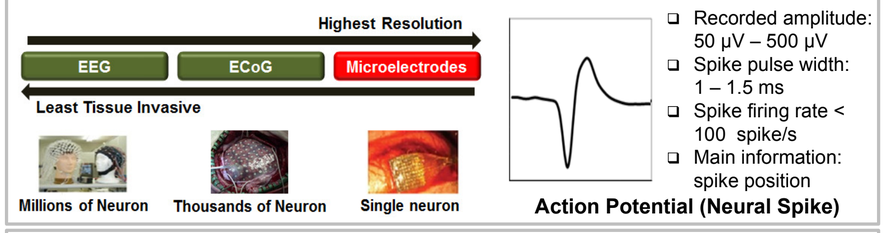
Introduction

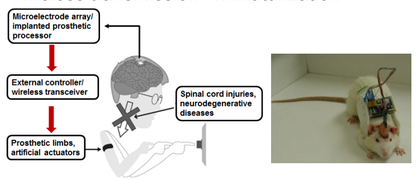
Monitoring Brain Activity



- Recorded amplitude: 50 µV – 500 µV
- Spike pulse width: 1 – 1.5 ms
- Spike firing rate < 100 spike/s
- Main information: spike position

Motivation and Challenge

- Neural recording for neural prostheses/research
- Wireless transmission / miniaturization

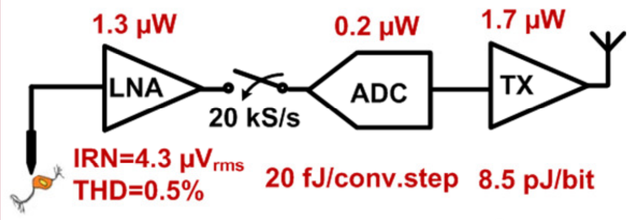


- Limited energy resources due to the required small form factor
- Sensitive environment which limits the maximum power density < 0.2 mW/mm^2
- Demand to increase the number of the recording channels, which increases the data rate: 100 x 20 kS/s x 10-bit = 20 Mb/s
- Low input-referred noise < 4 μV_{rms}

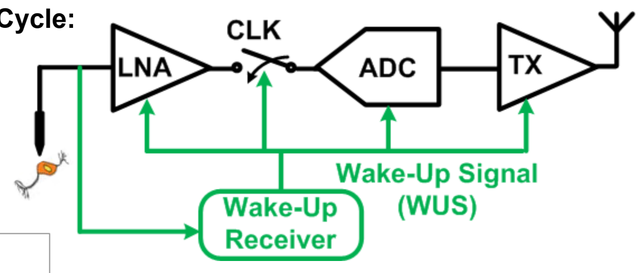
Objective: Design a *low power* 100-channel neural recording system with wireless telemetry

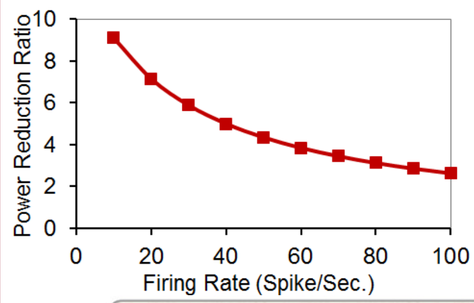
Power Reduction: Wake-Up Duty Cycling

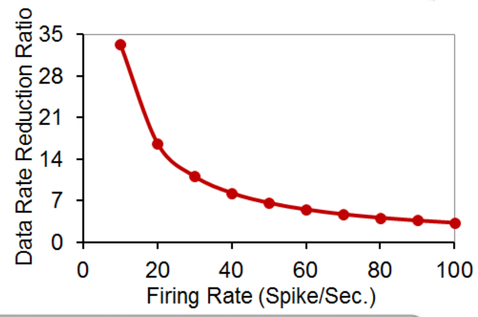
Typical Circuits in Neural Recording (Bio-Sensor)

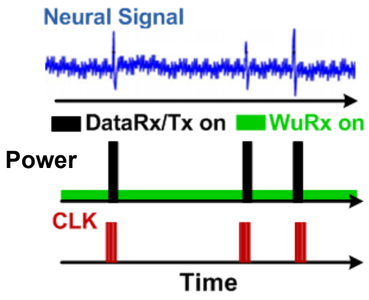


Information Duty Cycle: 3-30%





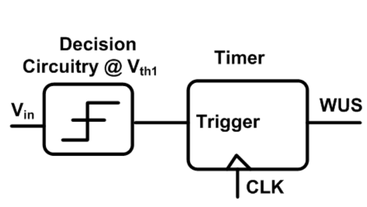


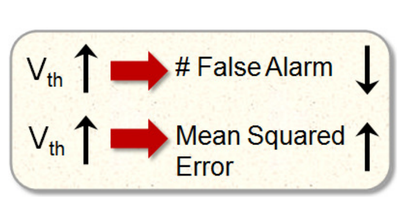


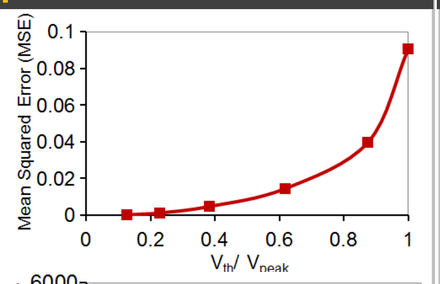
Key approach: Activate front-end module and transmitter only for action potentials, with a low power/sensitive wake-up receiver

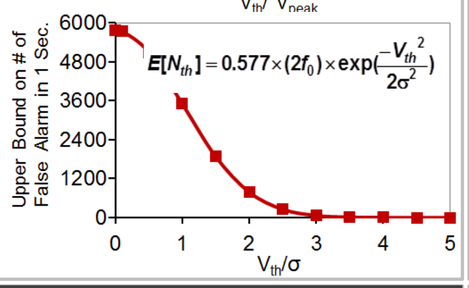
Wake-Up Receiver Scheme

Single-Threshold Wake-Up RX

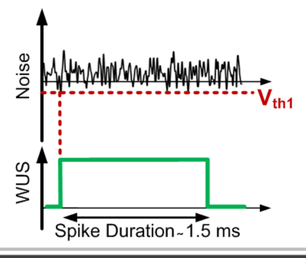




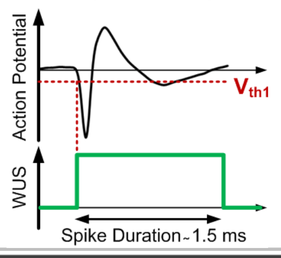




Response to Noise

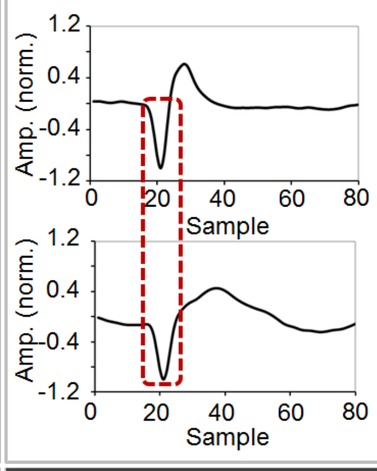


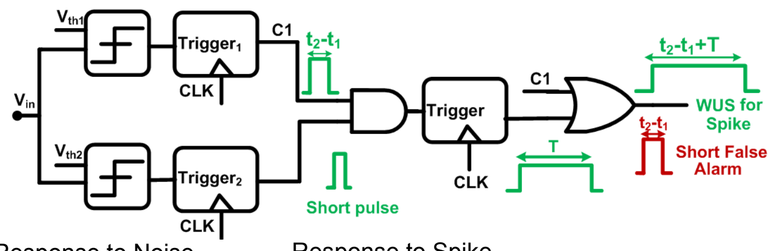
Response to Spike



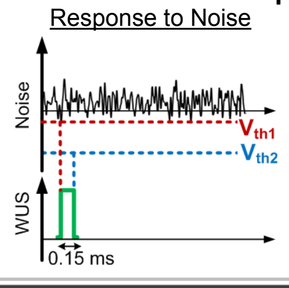
Dual-Threshold Wake-Up RX

Exploiting Spike Shape

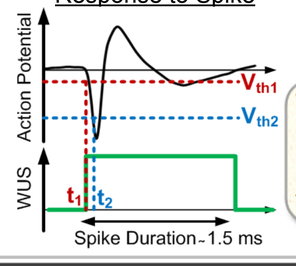




Response to Noise

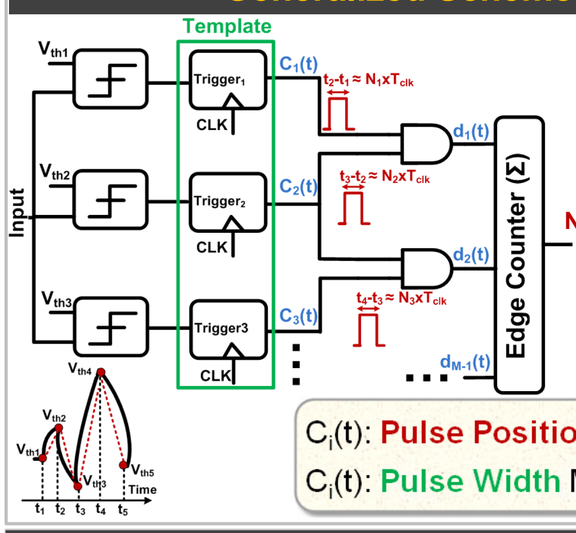


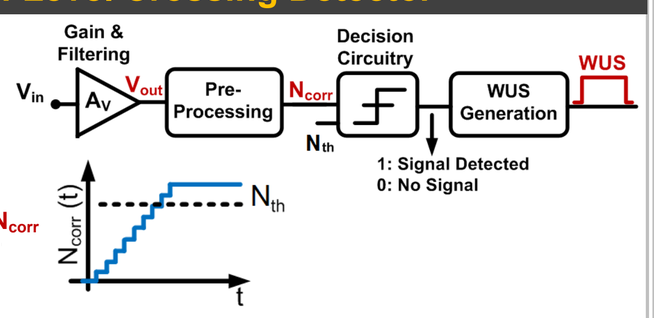
Response to Spike



The common feature of action potentials is used to shorten false alarm duration.

Generalized Scheme: Level Crossing Detector



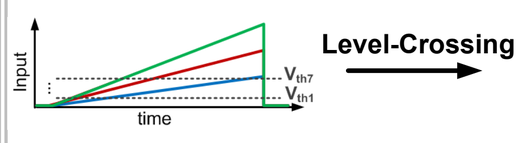


$$N_{corr}(t) = \sum_{i=1}^{M-1} d_i(t) = \sum_{i=1}^{M-1} C_i(t) C_{i+1}(t)$$

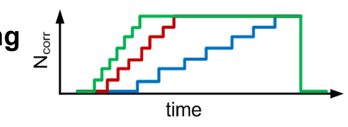
$C_i(t)$: **Pulse Position** Modulated by the **Input** Signal

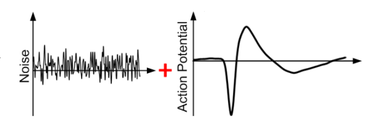
$C_i(t)$: **Pulse Width** Modulated by the **Template** Signal

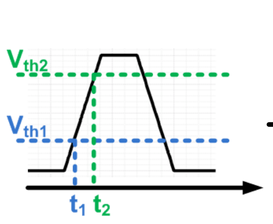
SNR Improvement for Higher Amplitude



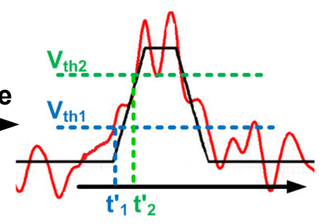
Level-Crossing





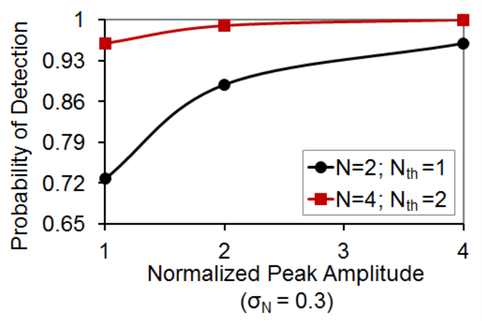


Noise

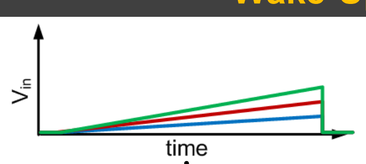


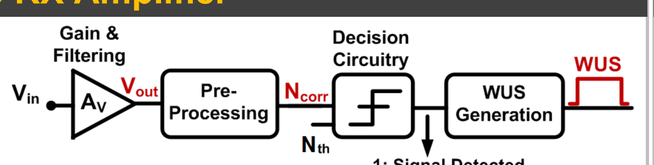
$$\sigma_t = \sigma_N \Big/ \frac{dV}{dt}$$

Amplitude ↑ → $\frac{dV}{dt}$ ↑ → σ_t ↓

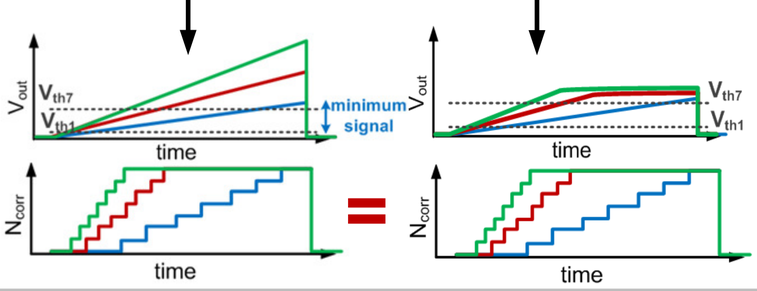


Wake-Up RX Amplifier





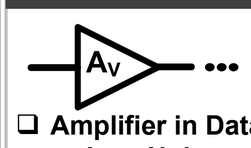
Linear A_V | Non-Linear A_V



Amplifier *linearity* is relaxed by using *level-crossing* detector as pre-processing.

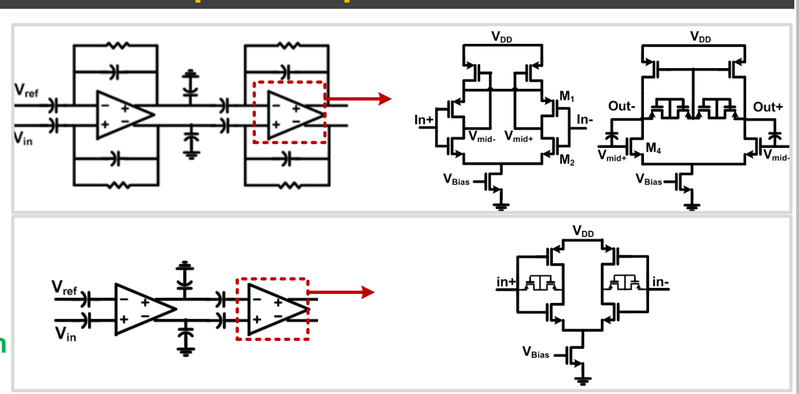
V_{DD}, I_{DC}, P_{DC} ↓

Data RX/Wake-Up RX Amplifiers



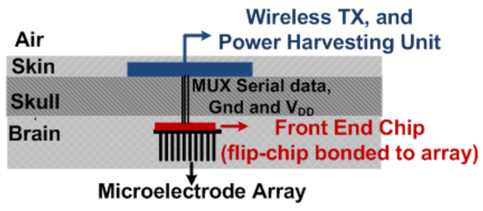
- **Amplifier in Data RX Path**
  - Low Noise
  - High Linearity
  - High Gain

- **Amplifier in Wake-Up RX Path**
  - Moderate Noise
  - Low Linearity
  - Moderate Gain

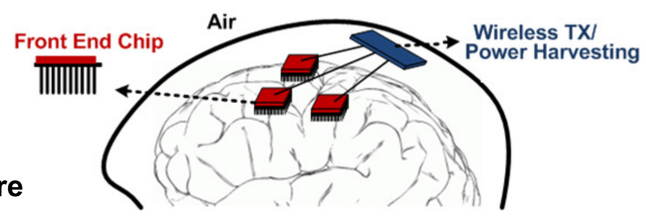


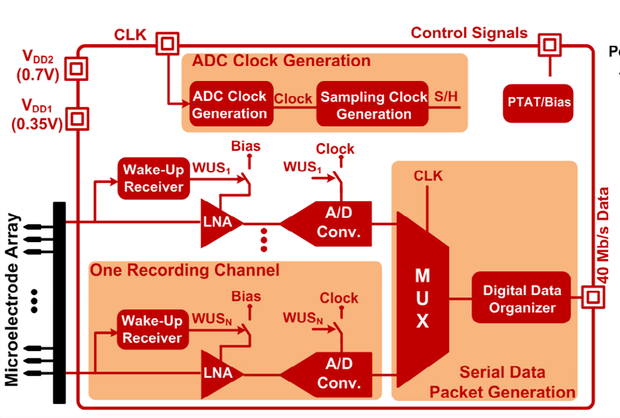
	Gain (dB)	Input Ref. Noise	THD (1 mV@1 kHz)	VDD (V)	Power (µW)
Data Rx	57	1.27 μV_{rms}	0.47%	0.7	2.13
Wake-up RX	53	2.1 μV_{rms}	90%	0.35	0.14

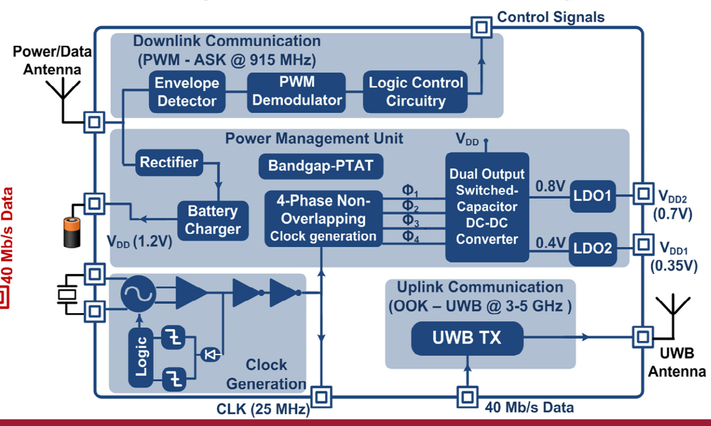
100-Channel Event-Driven Neural Recording System



Modular Architecture







Architecture Highlights

- Activity-dependent power consumption using low-power/sensitive wake-up RX
- Low-voltage and low-power design
  - Wake-up/ADC/Digital V_{DD}: 0.35 V
  - Neural Amplifier V_{DD}: 0.7 V
- Dual-chip neural recording system
  - More space for external components
  - Power distribution over larger volume
  - Modular architecture
- Dual-band wireless
  - 915 MHz for power telemetry
  - 3-5 GHz for data telemetry
- Separate 10-bit area/power-efficient SAR ADC for each channel
- Dual output, capacitance sharing switched-capacitor DC-DC converter
- Power efficient clock generation

Performance Summary

	ISSCC 2007	ISSCC 2008	TBCAS 2011	JSSCC 2012	This Work
No. of channel	100	128	32	96	100
Input-Ref. Noise	4.8 μV_{rms}	4.9 μV_{rms}	5.4 μV_{rm}	2.2 μV_{rm}	1.5 μV_{rms}
ADC (bits)	10	9	8	10	10
Wireless TX	Y	Y	N	N	Y
TX Data Rate	157 kb/s	90 Mb/s	-	-	40 Mb/s
Power	8 mW	6 mW	0.32 mW	6.5 mW	< 0.5 mW
Power/ channel	80 µW	46 µW	10 µW	67 µW	< 5 µW
Tech. (µm)	0.6	0.35	0.18	0.13	0.13

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