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Introduction

Monitoring Brain Activity

Recorded amplitude: 50 μV – 500 μV
Spike pulse width: 1 – 1.5 ms
Spike firing rate < 100 spike/s
Main information: spike position

Motivation and Challenge

- Neural recording for neural prostheses/research
- Wireless transmission / miniaturization
- Limited energy resources due to the required small form factor
- Sensitive environment which limits the maximum power density < 0.2 mW/mm²
- Demand to increase the number of the recording channels, which increases the data rate: 100 x 20 kS/s x 10-bit = 20 Mb/s
- Low input-referred noise < 4 μV_{rms}

Objective: Design a low power 100-channel neural recording system with wireless telemetry

Power Reduction: Wake-Up Duty Cycling

Typical Circuits in Neural Recording (Bio-Sensor)

1.3 μW (LNA), 0.2 μW (ADC), 1.7 μW (TX)

Information Duty Cycle: 3-30%

IRN=4.3 μV_{rms} , THD=0.5%, 20 kS/s, 20 fJ/conv.step, 8.5 pJ/bit

Key approach: Activate front-end module and transmitter only for action potentials, with a low power/sensitive wake-up receiver

Wake-Up Receiver Scheme

Single-Threshold Wake-Up RX

Response to Noise: Shows false alarms triggered by noise above Vth1.

Response to Spike: Shows correct detection of a spike above Vth1.

Mean Squared Error (MSE) vs Vth1/Vpeak

Upper Bound on # of False Alarm in 1 Sec. vs Vth1/σ

$$E[N_{fa}] = 0.577 \times (2f_0) \times \exp\left(-\frac{V_{th}^2}{2\sigma^2}\right)$$

Dual-Threshold Wake-Up RX

Exploiting Spike Shape: Shows how the spike's shape is used to distinguish it from noise.

Response to Noise: Shows no false alarms as noise does not reach the second threshold Vth2.

Response to Spike: Shows correct detection as the spike reaches both thresholds.

The common feature of action potentials is used to shorten false alarm duration.

Generalized Scheme: Level Crossing Detector

Gain & Filtering: $V_{in} \rightarrow A_v \rightarrow V_{out}$

Pre-Processing: N_{corr}

Decision Circuitry: 1: Signal Detected, 0: No Signal

WUS Generation

Edge Counter (Σ): $N_{corr}(t) = \sum_{i=1}^{M-1} d_i(t) = \sum_{i=1}^{M-1} C_i(t)C_{i+1}(t)$

$C_i(t)$: Pulse Position Modulated by the Input Signal
 $C_i(t)$: Pulse Width Modulated by the Template Signal

SNR Improvement for Higher Amplitude

Level-Crossing: Shows how multiple level crossings improve detection probability.

Probability of Detection vs Normalized Peak Amplitude ($\sigma_N = 0.3$)

Amplitude $\uparrow \rightarrow \frac{dV}{dt} \uparrow \rightarrow \sigma_t \downarrow$

Wake-Up RX Amplifier

Linear A_v vs Non-Linear A_v

Amplifier linearity is relaxed by using level-crossing detector as pre-processing.

$V_{DD}, I_{DC}, P_{DC} \downarrow$

Data RX/Wake-Up RX Amplifiers

- Amplifier in Data RX Path: Low Noise, High Linearity, High Gain
- Amplifier in Wake-Up RX Path: Moderate Noise, Low Linearity, Moderate Gain

	Gain (dB)	Input Ref. Noise	THD (1 mV@1 kHz)	VDD (V)	Power (μW)
Data Rx	57	1.27 μV_{rms}	0.47%	0.7	2.13
Wake-up RX	53	2.1 μV_{rms}	90%	0.35	0.14

100-Channel Event-Driven Neural Recording System

Wireless TX, and Power Harvesting Unit

Air

Skin

Skull

Brain

MUX Serial data, Gnd and VDD

Front End Chip (flip-chip bonded to array)

Microelectrode Array

Modular Architecture

Front End Chip

Air

Wireless TX/ Power Harvesting

Downlink Communication (PWM - ASK @ 915 MHz)

Envelope Detector, PWM Demodulator, Logic Control Circuitry

Power Management Unit

Rectifier, Bandgap-PTAT, Dual Output Switched-Capacitor DC-DC Converter, 4-Phase Non-Overlapping Clock generation, Battery Charger

Uplink Communication (OOK - UWB @ 3-5 GHz)

UWB TX

Control Signals

ADC Clock Generation, Clock Sampling Clock S/H Generation, PTAT/Bias

Wake-Up Receiver, LNA, A/D Conv., MUX, Digital Data Organizer, Serial Data Packet Generation

One Recording Channel

Wake-Up Receiver, LNA, A/D Conv., MUX

CLK (25 MHz), 40 Mb/s Data

Architecture Highlights

- Activity-dependent power consumption using low-power/sensitive wake-up RX
- Low-voltage and low-power design - Wake-up/ADC/Digital VDD: 0.35 V - Neural Amplifier VDD: 0.7 V
- Dual-chip neural recording system - More space for external components - Power distribution over larger volume - Modular architecture
- Dual-band wireless - 915 MHz for power telemetry - 3-5 GHz for data telemetry
- Separate 10-bit area/power-efficient SAR ADC for each channel
- Dual output, capacitance sharing switched-capacitor DC-DC converter
- Power efficient clock generation

Performance Summary

	ISSCC 2007	ISSCC 2008	TBCAS 2011	JSSCC 2012	This Work
No. of channel	100	128	32	96	100
Input-Ref. Noise	4.8 μV_{rms}	4.9 μV_{rms}	5.4 μV_{rms}	2.2 μV_{rms}	1.5 μV_{rms}
ADC (bits)	10	9	8	10	10
Wireless TX	Y	Y	N	N	Y
TX Data Rate	157 kb/s	90 Mb/s	-	-	40 Mb/s
Power	8 mW	6 mW	0.32 mW	6.5 mW	< 0.5 mW
Power/channel	80 μW	46 μW	10 μW	67 μW	< 5 μW
Tech. (μm)	0.6	0.35	0.18	0.13	0.13

