Passive Subharmonic Generation Using Memoryless Nonlinear Circuits

Zahra Safarian, *Student Member, IEEE*, and Hossein Hashemi, *Senior Member, IEEE*

***Abstract*—A passive subharmonic generation and frequency downconversion method using a memoryless nonlinear circuit coupled to a linear passive resonator is presented. The frequency downconverter can be used to transfer the energy from a high-frequency signal to a lower frequency without requiring any dc power supply. In the synchronous mode, the passive downconverter acts as a self-powered frequency divider. The characteristics of the self-powered frequency downconverter have been studied analytically, and design tradeoffs have been shown for the specific case of a cross-coupled differential pair nonlinearity. As an example, a low-frequency prototype is implemented with discrete components. Analytical results and design procedures are verified in discrete and integrated prototypes.**

***Index Terms*—CMOS, frequency conversion, frequency divider, nonlinear circuits, oscillators, subharmonic generation.**

I. Introduction

PASSIVE frequency downconverters and subharmonic generators can transfer the energy from a high-frequency source to a lower frequency without dc power consumption. They can be particularly useful in low power and batteryless RF integrated systems.

It is well known that when a signal is passing through a nonlinear and/or time-varying system, harmonics of the signal are generated at the output, irrespective of the input signal amplitude. However, in order to generate the subharmonic of the signal at the output, the input amplitude or power needs to be larger than a certain threshold. This is a known fact in frequency dividers such as injection-locked or regenerative frequency dividers. The main known technique for a *passive* frequency division is parametric frequency downconversion and division in which a subharmonic frequency is generated by exciting a nonlinear circuitry with *memory* or reactance (usually a varactor). These reactances transfer the energy from an ac source to the load and are capable of transferring power from one frequency to another. The downconversion using a reactive element was first observed and reported by North [1]. Later on in 1956, Manley and Rowe presented a general set of equations that relates the average powers at different frequencies in an ideal nonlinear reactance, independent of the nonlinearity shape [2]. The operation principles and requirements of parametric subharmonic oscillation using the semiconductor varactors have been described in [3]. Since then, there have been several designs on parametric frequency dividers implemented on printed circuit board (PCB) using discrete components [4]–[11]. There have been a few recent publications that demonstrate integrated *RF* parametric frequency dividers and downconverters in a CMOS technology [12]–[14]. Subharmonic oscillations are also known in acoustic systems, where by applying a strong electric excitation greater than a certain threshold, subharmonics or fractional harmonics of the applied frequency are generated. As an example, such subharmonics have been observed and reported in quartz plates [15]–[18].

In this paper, a new method for passive subharmonic generation, utilizing a *memoryless* nonlinear core coupled to a linear passive resonator, is proposed in which the energy of a RF source transfers to a lower frequency without consuming dc power. This lower frequency can be synchronized to the frequency of the input source, enabling realization of a passive frequency divider. Section II illustrates the concept and the operation principle. Section III shows the derivation of the downconverter properties using nonlinear analysis, which is applied to an *LC*-tuned cross-coupled topology. Section IV demonstrates a few design examples. Specifically, a 130-nm CMOS integrated 12-GHz passive divide-by-2 is demonstrated [19]. Section V concludes this paper.

II. Frequency Conversion Using Memoryless Nonlinear Circuits

Memoryless nonlinear circuits combined with linear passives can be configured to generate frequencies that are different than the input frequency without the need for a dc power supply or consuming dc power. In other words, some or all of the energy of an input drive can be transferred to generating and sustaining new frequencies that may be synchronous or asynchronous with respect to the input frequency.

Consider the circuit shown in Fig. 1(a). A dc supply voltage, V_{DD}, biases the transistors by supplying a dc current through them. With a large enough dc current, the small-signal conductance looking into the cross-coupled transistors becomes more negative than the *LC* resonator loss, i.e., $G + (1/R_L) < 0$. This causes an oscillation startup, and ultimately, a steady-state sinusoid at the frequency of the *LC* resonator is sustained due to the nonlinearity of active devices.

Now, consider the circuit in Fig. 1(b) where the dc voltage supply is replaced with an ac sinusoidal voltage source at

Manuscript received July 03, 2012; revised September 20, 2012; accepted September 21, 2012. Date of publication November 19, 2012; date of current version December 13, 2012. This work was supported in part by Corning Inc. and the National Science Foundation (NSF). This paper is an expanded paper from the IEEE MTT-S International Microwave Symposium, Montreal, QC, Canada, June 17–22, 2012.

The authors are with the Department of Electrical Engineering–Electrophysics, University of Southern California, Los Angeles, CA 90089-0271 USA (e-mail: zsafaria@usc.edu; hosseinh@usc.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2012.2222657

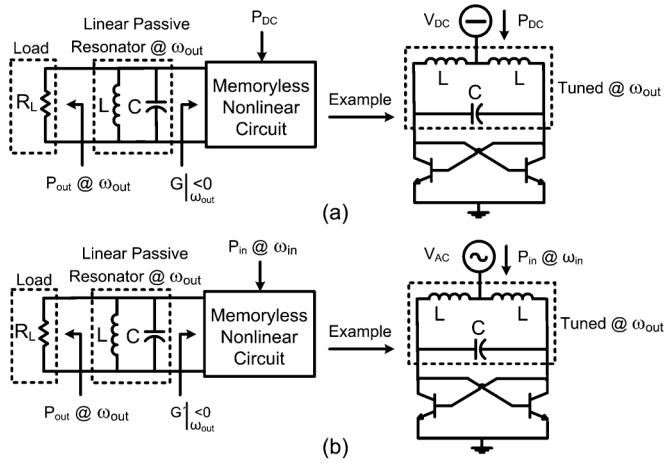


Fig. 1. (a) Negative resistance oscillator. (b) Proposed passive subharmonic generator using memoryless nonlinear circuitry.

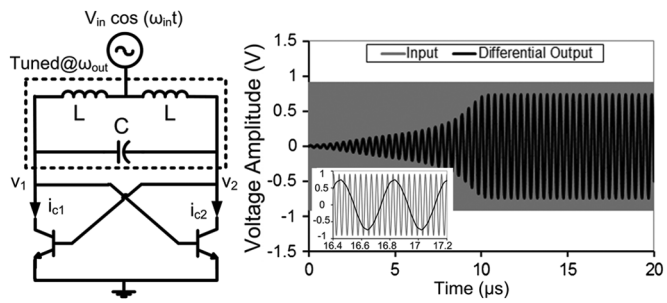


Fig. 2. Input/output voltage waveforms when $f_{\rm in} = 26.4$ MHz and $f_{\rm out} = 2.64$ MHz ($f_{\rm in} = 10 f_{\rm out}$); $L = 2.2$ μH, $Q = 13$, and $C = 820$ pF. A zoomed version is shown in the inset.

frequency $\omega_{\rm in}$. We will show that, under the right conditions, this circuit can generate a steady-state sinusoidal output at frequency $\omega_{\rm out} < \omega_{\rm in}$. In fact, we will show that there is no need for dc current through the transistors to generate this output (Section IV-C). Output frequency $\omega_{\rm out}$ can be independent of the input frequency (asynchronous operation) or a subharmonic of the input frequency (synchronous operation).

Fig. 2 shows a representative simulation of the circuit in the synchronous mode where $\omega_{\rm in} = 10\omega_{\rm out}$. We hypothesize that the voltage waveform across a high quality factor resonator primarily contains frequency $\omega_{\rm out}$, the resonant frequency of the passive *LC*. Since the input signal at frequency $\omega_{\rm in}$ is applied to a common mode of this circuit, we further hypothesize that the single-ended voltages across this circuit can be written as

$$\begin{aligned} v_1 &= \frac{1}{2} v_d \cos(\omega_{\rm out} t) + v_c \cos(\omega_{\rm in} t + \theta) \\ v_2 &= \frac{1}{2} v_d \cos(\omega_{\rm out} t + \pi) + v_c \cos(\omega_{\rm in} t + \theta) \end{aligned} \tag{1}$$

where v_d and v_c are the differential and common mode voltage amplitudes, respectively, and θ is the phase angle between the two signals. The collector currents in the bipolar junction transistors (BJTs) can then be expressed as

$$\begin{aligned} i_{c1} &\approx I_s e^{\frac{v_d}{2V_T}\cos(\omega_{\rm out} t)} \times e^{\frac{v_c}{V_T}\cos(\omega_{\rm in} t + \theta)} \\ i_{c2} &\approx I_s e^{\frac{-v_d}{2V_T}\cos(\omega_{\rm out} t)} \times e^{\frac{v_c}{V_T}\cos(\omega_{\rm in} t + \theta)} \end{aligned} \tag{2}$$

where I_s is the saturation current of the identical BJTs and V_T is the thermal voltage. The exponential of a cosinusoidal function can be expressed as [20]

$$e^{\pm x\cos(\omega t)} = I_0(\pm x) + 2\sum_{k=1}^{\infty} I_k(\pm x)\cos(k\omega t) \tag{3}$$

where $I_k(.)$ is the modified Bessel function of the first kind and order k. Since modified Bessel functions of odd (even) order are odd (even) functions of their argument [20], the differential current across the active circuitry can be written as

$$\begin{aligned} i_d =& i_{c2} - i_{c1} \\ =& -4I_s \Bigg\{ I_0(\alpha) \sum_{k=1}^{\infty} I_{2k-1}(\beta)\cos\left((2k-1)\omega_{\rm out} t\right) \\ &+ \sum_{k=1}^{\infty}\sum_{m=1}^{\infty} I_m(\alpha)\left[\cos\left[\left((2k-1)\omega_{\rm out} + m\omega_{\rm in}\right)t + m\theta\right]\right. \\ &\left. + \cos\left[\left((2k-1)\omega_{\rm out} - m\omega_{\rm in}\right) \cdot t - m\theta\right]\right] I_{2k-1}(\beta) \Bigg\} \end{aligned} \tag{4}$$

where $\alpha = v_c/V_T$ and $\beta = v_d/2V_T$ are the normalized common mode and differential voltages, respectively. In order to simplify the analysis, we consider the synchronous mode and assume that $\omega_{\rm in} = n\omega_{\rm out}$, where n is an integer number. Therefore, $i_d(\omega_{\rm out})$ can be derived as

$$\begin{aligned} i_d(\omega_{\rm out}) = -4I_s \Bigg[& I_1(\beta) I_0(\alpha)\cos(\omega_{\rm out} t) + \sum_{m=1}^{\infty} I_m(\alpha) \\ & \times \left(I_{mn-1}(\beta) + I_{mn+1}(\beta)\right)\cos(\omega_{\rm out} t - m\theta) \Bigg] \end{aligned} \tag{5}$$

where only odd terms of $I_{mn-1}(\beta)$ and $I_{mn+1}(\beta)$ should be considered. Now, we can find the equivalent input admittance of the the active circuitry at frequency $\omega_{\rm out}$ by taking the ratio of the differential current component at $\omega_{\rm out}$ to the differential voltages as

$$\begin{aligned} G' &= \frac{i_d(\omega_{\rm out})}{v_1 - v_2} \\ &= \frac{-2I_s}{\beta V_T}\left[I_1(\beta) I_0(\alpha) + \sum_{m=1}^{\infty} I_m(\alpha)\left(I_{mn-1}(\beta) + I_{mn+1}(\beta)\right) \right] \end{aligned} \tag{6}$$

where $\theta \simeq 0$ is assumed for simplicity. It is easy to see that $G' < 0$ since the modified Bessel functions I_k are positive for positive arguments. Intuitively, this negative conductance enables starting and sustaining steady-state oscillation at $\omega_{\rm out}$. This intuitive reasoning will be concretely substantiated in Section III.

III. Analysis

This section covers the analysis and simulation results of the passive frequency conversion scheme of Fig. 2.

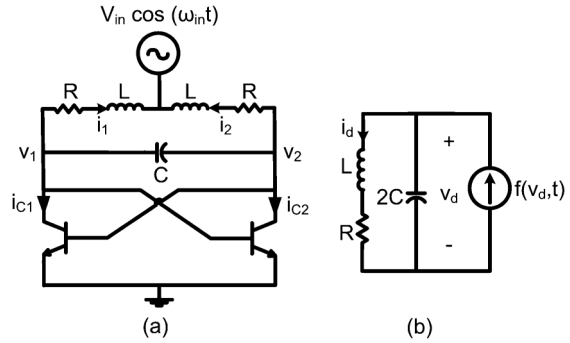


Fig. 3. (a) Self-powered downconverter with state-variables. (b) Second-order model for the downconverter.

A. Formulation and Analytical Approach

Let us assume v_1, v_2, i_1, and i_2 represent the single-ended output voltages and inductor currents, respectively [see Fig. 3(a)]. The input signal is also $V_{\rm in}\cos(\omega_{\rm in}t)$. Neglecting base currents in the BJTs, the following equations can be written:

$$\begin{aligned} C\dot{v_1} - C\dot{v_2} &= -i_1 - i_{c1} \\ C\dot{v_2} - C\dot{v_1} &= -i_2 - i_{c2} \\ L\dot{i_1} &= -Ri_1 + v_1 - V_{\rm in}\cos(\omega_{\rm in}t) \\ L\dot{i_2} &= -Ri_2 + v_2 - V_{\rm in}\cos(\omega_{\rm in}t) \\ i_{c1} &\approx I_s e^{\frac{v_2}{V_T}} \\ i_{c2} &\approx I_s e^{\frac{v_1}{V_T}}. \end{aligned} \tag{7}$$

Taking the independent state variables as $v_d = v_1 - v_2$, $i_c = i_1 + i_2$, and $i_d = i_1 - i_2$, the set of differential equations for the system is

$$\begin{bmatrix} \dot{i_d} \\ \dot{v_d} \\ \dot{i_c} \end{bmatrix} = \begin{bmatrix} \frac{-R}{L} & \frac{1}{L} & 0 \\ \frac{-1}{2C} & 0 & 0 \\ 0 & 0 & \frac{-R}{L} \end{bmatrix} \begin{bmatrix} i_d \\ v_d \\ i_c \end{bmatrix} + F(v_d, i_c, t) \tag{8}$$

where $F(i_c, v_d, t)$ is a time-varying nonlinear function vector given by

$$\begin{bmatrix} 0 \\ \frac{-i_c}{2C} \times \tanh\left(\frac{v_d}{2V_T}\right) \\ \frac{-2V_{\rm in}}{L}\cos(\omega_{\rm in}t) + \frac{2V_T}{L}\ln\left(\frac{-i_c}{2I_s}\operatorname{sech}\left(\frac{v_d}{2V_T}\right)\right) \end{bmatrix}. \tag{9}$$

Thus, the dynamics of the circuit is described by a third-order nonautonomous nonlinear differential equation, where the differential voltage v_d and current i_d depend on the common-mode current i_c. Some simplifying assumptions will be made in order to solve this equation, the validity of which will be verified with simulations, and ultimately, measurements.

Assuming zero initial conditions for the inductor and capacitor, at $t = 0$, v_1 and v_2 are equal to the common mode input voltage. Therefore, at $t = 0$, $v_c = v_1 + v_2 = 2V_{\rm in}\cos(\omega_{\rm in}t)$, and thus,

$$\begin{aligned} i_c &= i_1 + i_2 \\ &= -(i_{c1} + i_{c2}) \\ &= -2I_s e^{\frac{V_{\rm in}}{V_T}\cos(\omega_{\rm in}t)}. \end{aligned} \tag{10}$$

For $t > 0$, while the differential voltage v_d is still small, we assume that the common mode voltage, v_c, and common mode current, i_c, remain approximately intact. With the approximate solution for i_c, the differential equations in (8) simplify to

$$\begin{bmatrix} \dot{i_d} \\ \dot{v_d} \end{bmatrix} = \begin{bmatrix} \frac{-R}{L} & \frac{1}{L} \\ \frac{-1}{2C} & 0 \end{bmatrix} \begin{bmatrix} i_d \\ v_d \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{2C}f(v_d, t) \end{bmatrix} \tag{11}$$

where $f(v_d, t) = 2I_s e^{(V_{\rm in}/V_T)\cos(\omega_{\rm in}t)}\tanh(v_d/2V_T)$. Thus, the dynamics of the circuit is governed by a second-order nonautonomous nonlinear differential equation. In this case, the circuit can be modeled as an *RLC* tank with the capacitor voltage and inductor current (v_d and i_d) as state variables and a nonlinear time-dependent current source $f(v_d, t)$ that represents the differential current $(i_{c2} - i_{c1})$ in the transistor pair [see Fig. 3(b)].

In order to derive the transient waveforms, quasi-harmonic approximation is used, where the transient and steady-state expressions for the voltage and current waveforms are assumed to resemble sinusoids with slowly time-varying amplitude $r(t)$ and phase $\phi(t)$ as [21]

$$\begin{aligned} v_d(t) &= r(t)\cos\left(\omega_{\rm out}t + \phi(t)\right) \\ i_d(t) &= 2\omega_{\rm out}C \times r(t)\sin\left(\omega_{\rm out}t + \phi(t)\right) \end{aligned} \tag{12}$$

and $\omega_{\rm out} = 1/\sqrt{2LC}$. The quasi-harmonic approximation is valid as long as the *RLC* quality factor is reasonably large. By taking the derivatives of v_d and i_d in (12) with respect to time and replacing them in the original equation [see (11)], the following first-order differential equations for $r(t)$ and $\phi(t)$ are obtained:

$$\begin{aligned} \dot{r} &= \frac{1}{2C}f\left(r\cos(\omega_{\rm out}t + \phi), t\right) \cdot \cos(\omega_{\rm out}t + \phi) \\ &\quad + \frac{-R}{L}r\sin^2(\omega_{\rm out}t + \phi) \\ \dot{\phi} &= \frac{-1}{2Cr}f\left(r\cos(\omega_{\rm out}t + \phi), t\right) \cdot \sin(\omega_{\rm out}t + \phi) \\ &\quad + \frac{-R}{2L}r\sin(2\omega_{\rm out}t + 2\phi) \end{aligned} \tag{13}$$

where

$$\begin{aligned} f\left(r\cos(\omega_{\rm out}t + \phi), t\right) &= 2I_s \exp\left(\frac{V_{\rm in}}{V_T}\cos(\omega_{\rm in}t)\right) \\ &\quad \times \tanh\left(\frac{r}{2V_T}\cos(\omega_{\rm out}t + \phi)\right). \end{aligned} \tag{14}$$

In order to convert the above nonautonomous differential equations to autonomous ones (i.e., remove explicit time dependency), the equations are averaged over one oscillation period,

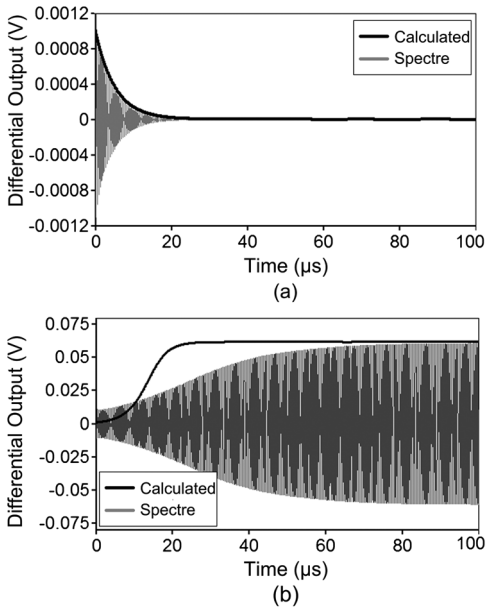


Fig. 4. Transient behavior of the circuitry for: (a) $V_{\rm in} = 0.68$ V and (b) $V_{\rm in} = 0.7$ V.

$T = 2\pi/\omega_{\rm out}$. Since the amplitude and the phase are slowly varying functions of time over the oscillation period, they are assumed to be constant in the averaging process. Therefore, the *averaged* differential equations for $r(t)$ and $\phi(t)$ are given by

$$\dot{\bar{r}} = \frac{1}{2C}\cdot\frac{1}{T}\int_T f\left(r\cos(\omega_{\rm out}t\phi), t\right)\cos(\omega_{\rm out}t+\phi)dt + \frac{-R}{2L}r$$
$$\dot{\bar{\phi}} = \frac{-1}{2Cr}\cdot\frac{1}{T}\int_T f\left(r\cos(\omega_{\rm out}t+\phi), t\right)\sin(\omega_{\rm out}t+\phi)dt. \quad (15)$$

In steady state, the amplitude and phase variations should be zero, i.e., $\dot{\bar{r}} = 0$ and $\dot{\bar{\phi}} = 0$. Fig. 4(a) shows the numerical solution of (15) using MATLAB and the simulated transient voltage waveform using Spectre for the differential voltage v_d when $V_{\rm in} = 0.68$ V. Fig. 4(b) shows the same graphs when $V_{\rm in} = 0.7$ V. Analysis and transient simulations consistently show growth and sustaining of a sinusoidal differential voltage for large input amplitudes, and zero differential output for small input voltages. Throughout this section, the BJT model used for calculations and simulations is PBR951 UHF wideband transistor with $I_s = 0.963$ fA and $\beta = 102$. All the simulations and calculations are performed for $L = 2.2$ μH and $C = 820$ pF, corresponding to a tuned frequency of approximately 2.64 MHz, and $R = 2.8\ \Omega$, corresponding to the inductor quality factor of 13 at 2.64 MHz.

B. Startup Condition—Synchronous Mode

In this section, we find the minimum required input amplitude $V_{\rm in,th}$ that causes growth of differential output voltage. To find a closed-form formula for the startup condition, the $\tanh(.)$ function in (15) is approximated with the first two terms of its Taylor-series expansion, i.e., $\tanh(x) \approx x - x^3/3$. To simplify the analysis, we also assume that the input frequency is an integer multiple of output frequency, i.e., $\omega_{\rm in} = n\omega_{\rm out}$, where n is an integer. The following averaged autonomous nonlinear differential equations for the amplitude $\dot{\bar{r}}$ and phase $\dot{\bar{\phi}}$ can be found for different values of n.

1) $n = 1$:

$$\dot{\bar{r}} = r\left\{\frac{-R}{2L} + \frac{I_s}{4CV_T}\left[I_0(\alpha) + I_2(\alpha)\cos(2\phi)\right]\right\} - \left(\frac{r}{2V_T}\right)^3 \times \frac{I_s}{2C}\left[\frac{3}{4}I_0(\alpha) + I_2(\alpha)\cos(2\phi) + \frac{1}{4}I_4(\alpha)\cos(4\phi)\right]$$
$$\dot{\bar{\phi}} = \frac{-I_s\sin(2\phi)}{4CV_T}\left[I_2(\alpha) - \left(\frac{r}{2V_T}\right)^2 \times \left(\frac{I_2(\alpha)}{2} + \frac{I_4(\alpha)}{2}\cos(2\phi)\right)\right]. \quad (16)$$

2) $n = 2$:

$$\dot{\bar{r}} = r\left\{\frac{-R}{2L} + \frac{I_s}{4CV_T}\left[I_0(\alpha) + I_1(\alpha)\cos(2\phi)\right]\right\} - \left(\frac{r}{2V_T}\right)^3 \times \frac{I_s}{2C}\left[\frac{3}{4}I_0(\alpha) + I_1(\alpha)\cos(2\phi) + \frac{1}{4}I_2(\alpha)\cos(4\phi)\right]$$
$$\dot{\bar{\phi}} = \frac{-I_s\sin(2\phi)}{4CV_T}\left[I_1(\alpha) - \left(\frac{r}{2V_T}\right)^2 \times \left(\frac{I_1(\alpha)}{2} + \frac{I_2(\alpha)}{2}\cos(2\phi)\right)\right]. \quad (17)$$

3) $n = 4$:

$$\dot{\bar{r}} = r\left[\frac{-R}{2L} + \frac{I_s}{4CV_T}I_0(\alpha)\right] - \frac{I_s}{2C}\left(\frac{r}{2V_T}\right)^3\left[\frac{3}{4}I_0(\alpha) + \frac{1}{4}\times I_1(\alpha)\cos(4\phi)\right]$$
$$\dot{\bar{\phi}} = \frac{I_sI_1(\alpha)}{16CV_T}\left(\frac{r}{2V_T}\right)^2\sin(4\phi). \quad (18)$$

4) $n = 3$ and $n \geq 5$:

$$\dot{\bar{r}} = r\left[\frac{-R}{2L} + \frac{I_s}{4CV_T}I_0(\alpha)\right] - \frac{3I_s}{8C}\left(\frac{r}{2V_T}\right)^3 I_0(\alpha)$$
$$\dot{\bar{\phi}} = 0. \quad (19)$$

By definition, the amplitude and phase variation should be zero in the steady state, i.e., $\dot{\bar{r}} = 0$ and $\dot{\bar{\phi}} = 0$. Stability analysis of steady-state solutions offers the following startup condition for the batteryless driven nonlinear circuit of Fig. 3 (details in the Appendix):

$$n = 1: \ \frac{I_s\left[I_0(\alpha) + I_2(\alpha)\right]}{V_T} > \frac{2RC}{L}$$
$$n = 2: \ \frac{I_s\left[I_0(\alpha) + I_1(\alpha)\right]}{V_T} > \frac{2RC}{L}$$
$$n \geq 3: \ \frac{I_sI_0(\alpha)}{V_T} > \frac{2RC}{L}. \quad (20)$$

Since $I_1(.) > I_2(.) > 0$, $n = 2$ requires the minimum $\alpha = V_{\rm in}/V_T$ to satisfy the startup condition. Furthermore, for $n \geq 3$, the startup condition remains constant for all values of n.

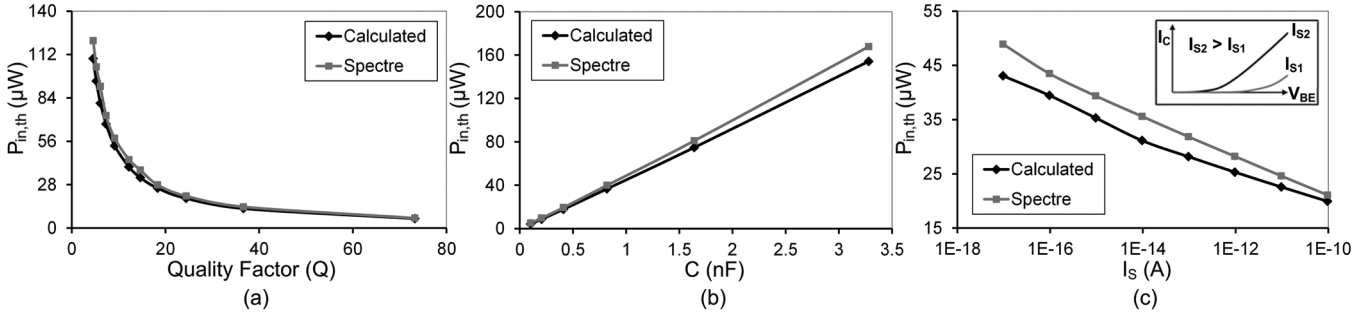


Fig. 5. Minimum required input power for startup $P_{\mathrm{in,th}}$ when $n = \omega_{\mathrm{in}}/\omega_{\mathrm{out}} = 2$ versus: (a) resonator quality factor Q, (b) resonator capacitance C, and (c) BJT saturation current I_S.

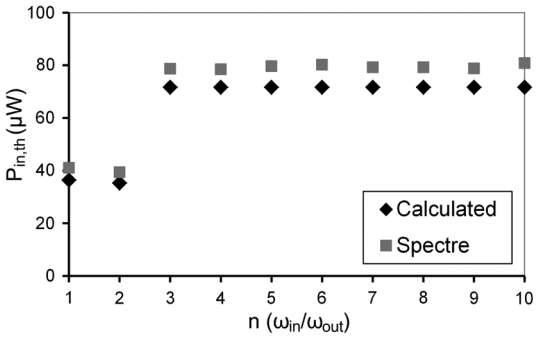


Fig. 6. Minimum required input power for startup $P_{\mathrm{in,th}}$ versus $n = \omega_{\mathrm{in}}/\omega_{\mathrm{out}}$ when $Q = 13$.

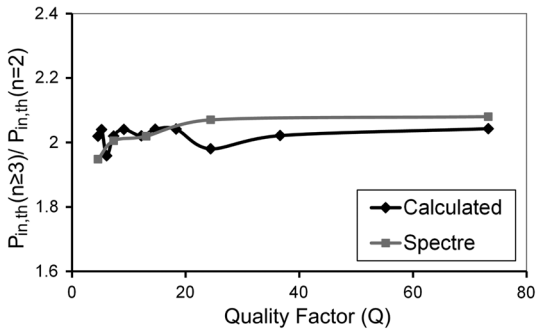


Fig. 7. Normalized minimum required input power for startup $P_{\mathrm{in,th}}(n \geq 3)/P_{\mathrm{in,th}}(n = 2)$ versus resonator quality factor (Q).

Oftentimes, it is desirable to find the circuit startup condition and other properties in terms of input power instead of input voltage swing. In the synchronous mode, the average input power is

$$P_{\mathrm{in}} = \frac{1}{T}\int_{T} V_{\mathrm{in}} \cos(\omega_{\mathrm{in}} t) \cdot i_c dt \tag{21}$$

where T is the largest period in the system. At startup and for small differential voltage, v_d, the common-mode current is given by (10). In this case, the input power is simplified to

$$P_{\mathrm{in}} \approx 2 I_s I_1(\alpha) V_{\mathrm{in}}. \tag{22}$$

Equations (20) and (22) can be combined to find the minimum input power $P_{\mathrm{in,th}}$ necessary to start a growing oscillation at $\omega_{\mathrm{out}} = \omega_{\mathrm{in}}/n$. Fig. 5(a) shows the calculated and Spectre simulated minimum required input power for startup $P_{\mathrm{in,th}}$ versus resonator quality factor (Q) for $n = 2$; higher resonator Q relaxes the startup condition. Fig. 5(b) shows $P_{\mathrm{in,th}}$ versus resonator capacitance, C. For this simulation, the Q of the tank is kept constant at $Q = 13$. Resonators with smaller C requires lower P_{in} for startup oscillation. This may be intuitively expected as, for the same Q, smaller capacitor corresponds to larger effective parallel resistance for the resonator. Fig. 5(c) shows $P_{\mathrm{in,th}}$ versus BJT saturation current I_s. For this simulation, only the parameter I_s in the model file of the BJT transistor PBR951 has been changed. The minimum required input power reduces as I_s increases corresponding to a steeper $I_c - V_{\mathrm{BE}}$ response and a smaller $V_{\mathrm{BE,ON}}$ for the BJTs. Fig. 6 shows $P_{\mathrm{in,th}}$ versus $n = \omega_{\mathrm{in}}/\omega_{\mathrm{out}}$ for $Q = 13$. As predicted by the calculations, $n = 2$ requires the minimum $P_{\mathrm{in,th}}$, and as n increases, $P_{\mathrm{in,th}}$ stays almost constant. Finally, Fig. 7 shows the ratio of $P_{\mathrm{in,th}}$ at $n \geq 3$ to $P_{\mathrm{in,th}}$ at $n = 2$ versus Q. This ratio is approximately 2, suggesting that the minimum required input power to start a synchronous output at $\omega_{\mathrm{out}} = \omega_{\mathrm{in}}/n$ for $n \geq 3$ is 3 dB more than that for $n = 2$, nearly independent of the quality factor.

C. Steady-State Solutions—Synchronous Mode

Nonzero steady-state amplitude and phase solutions $(r_{\mathrm{ss}}, \phi_{\mathrm{ss}})$ in the synchronous mode, i.e., the $n = \omega_{\mathrm{in}}/\omega_{\mathrm{out}}$ integer, are found by setting $\dot{r} = 0$ and $\dot{\phi} = 0$ in (15). Fig. 8(a) and (b) shows the variation of the steady-state amplitudes r_{ss} as V_{in}, and therefore, P_{in} varies for $n = 2$ and two different inductor Q values. As can be seen, by increasing P_{in}, v_d increases smoothly (power/current limited region) and saturates at a specific value where it does not increase by increasing input power (voltage limited region). Since in deriving (15), we have assumed that v_d has a relatively small amplitude, the calculation is not valid at large output swing values. As expected intuitively, oscillators with higher Q also requires smaller P_{in} to achieve a certain output swing. Fig. 8(c) shows the variation of the steady-state amplitudes r_{ss} as P_{in} varies for two different resonator capacitance C, while $n = 2$ and $Q = 13$. With smaller C, larger output swing for the same input power is achieved.

The output power is defined as the power delivered to R_L, the total parallel resistance of the tank (Fig. 1)

$$P_{\mathrm{out}} = \frac{r_{\mathrm{ss}}^2}{2R_L}. \tag{23}$$

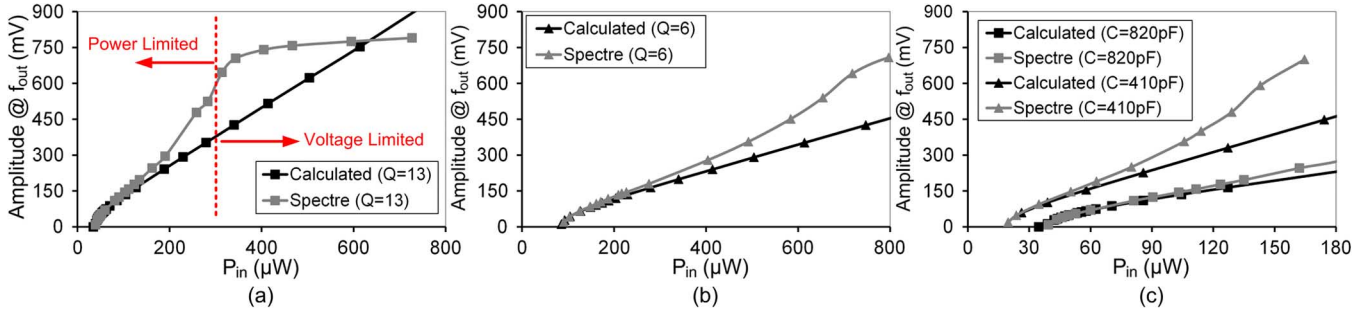


Fig. 8. Variation of the steady-state amplitudes r_{ss} as P_{in} varies for $f_{in} = 2f_{out} = 5.29$ MHz when: (a) $Q = 13$, (b) $Q = 6$, and (c) $C = 810$ pF and 410 pF.

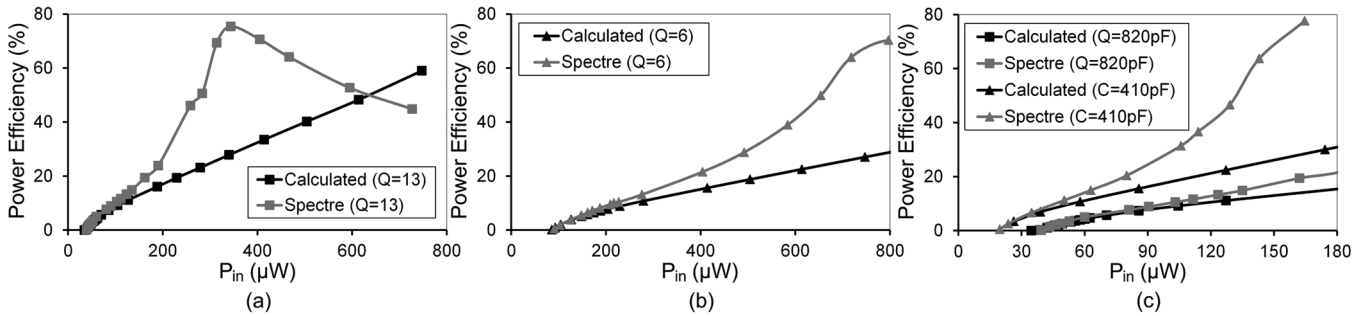


Fig. 9. Variation of the power efficiency η as P_{in} varies for $f_{in} = 2f_{out} = 5.29$ MHz when: (a) $Q = 13$, (b) $Q = 6$, and (c) $C = 810$ pF and 410 pF.

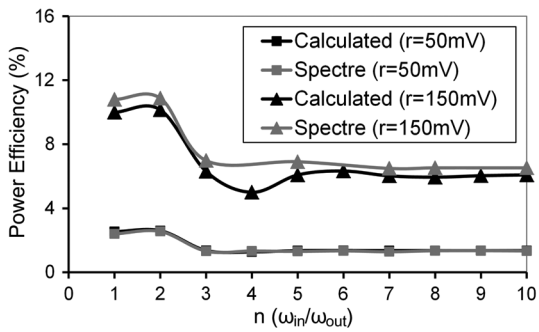


Fig. 10. Variation of the power efficiency η versus n for $r = 50$ mV and $r = 150$ mV when $Q = 13$.

This resistor captures the resonator loss, represented by $R_P = 2((L\omega_{out})^2/R)$, as well as any explicit load resistance. In an ideal case, the resonator should be lossless and the load resistance, to which the power is intended for delivery, is the only contributor to R_L. As such, all the references to the resonator quality factor are intended for the loaded quality factor. The power transfer efficiency can be derived as

$$\eta_p = \frac{P_{out}}{P_{in}}. \tag{24}$$

Fig. 9(a) and (b) shows power efficiency versus P_{in} for $n = 2$ and two different inductor Q values. We can observe that, in the power/current limited region, power efficiency increases as P_{in} increases. However, in the voltage-limited region, the efficiency drops by increasing P_{in}, since the output voltage is almost constant. Higher Q also results in higher efficiency. Fig. 9(c) shows power efficiency versus P_{in} for two different resonator capacitance C. Lower capacitance results in higher power transfer efficiency. Fig. 10 shows power efficiency versus n for different input voltage swing levels where n is assumed to be an integer number. The circuitry shows the highest efficiency at $n = 2$. As n increases, the efficiency does not change and it is almost half of the efficiency at $n = 2$.

D. *Effect of Detuning and Locking Range*

In practice, the passive resonator frequency may not be exactly equal to an integer frequency of input frequency, i.e., $\omega_{out} \neq (\omega_{in}/n)$. In this section, we derive the maximum frequency detuning for which the circuit still operates in the synchronous mode, i.e., it produces an output frequency that is exactly equal to ω_{in}/N, where N is an integer number. Let us assume $\omega_{in}/\omega_{out} = n = N + \delta$, where N is an integer and $\delta \ll N$ represents the frequency detuning. For $\delta \neq 0$, the output waveform may have different behaviors. At small input voltage levels, as n is detuned from integer values, the oscillation amplitude decreases until it dies [see Fig. 11(a)]. As the input amplitude increases, by detuning n, the oscillation amplitude decreases until it goes out of the locking range where it has an asynchronous oscillation with amplitude much smaller compared to the integer n [see Fig. 11(b)]. As input amplitude increases more, by detuning n, the oscillation amplitude does not change, saturated at approximately the maximum value; however, as it goes out of the locking range, it has an asynchronous oscillation with negligible change in the peak amplitude [see Fig. 11(c)].

Now we want to find the detuning range or the locking range. If the output signal is synchronized with the input signal, its frequency $\omega_{out} + \dot{\phi}$ will be equal to ω_{in}/N. For $\delta \ll N$, we assume that (16)–(19) can still represent the average equations for the system. In this case, $\bar{\dot{r}} = 0$ and $\bar{\dot{\phi}} = (\delta/N)\omega_{out}$ represent the steady-state locking condition.

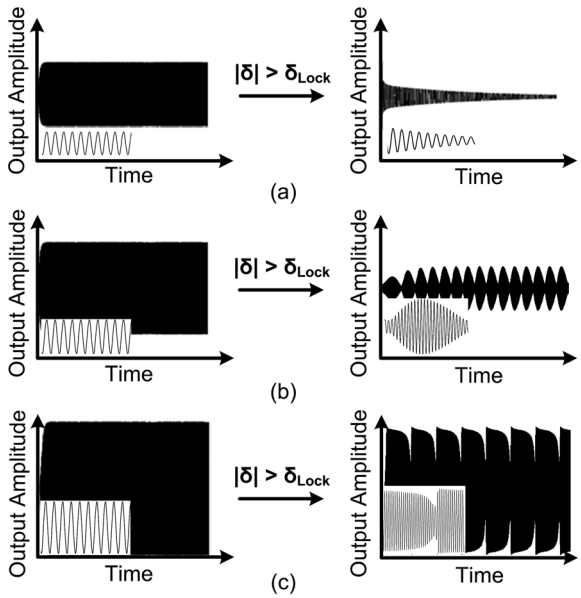


Fig. 11. Different scenarios for the oscillator output signal, when it is detuned more than it can tolerate at different $V_{\rm in}$: (a) $V_{\rm in1}$, (b) $V_{\rm in2}$, and (c) $V_{\rm in3}$, where $V_{\rm in1} < V_{\rm in2} < V_{\rm in3}$. Zoomed versions are shown in the respective insets.

The detailed analysis is going to be shown for $N = 2$. In this case, there are two fixed points, (r, ϕ). The first one is

$$r = 0$$
$$\frac{\delta}{2}\omega_{\rm out} = -\frac{I_s I_1(\alpha)}{4CV_T}\sin(2\phi) \tag{25}$$

corresponding to oscillator dying down [see Fig. 11(a)]. To find the stability of this fixed point, the averaged equation is linearized around the fixed point. In this case, the eigenvalues of the linearized equation are

$$\lambda_1 = \frac{-R}{2L} + \frac{I_s}{4CV_T}\left[I_0(\alpha) + I_1(\alpha)\cos(2\phi)\right]$$
$$\lambda_2 = \frac{-I_s I_1(\alpha)}{2CV_T}\cos(2\phi). \tag{26}$$

If n is an integer number ($\delta = 0$), ϕ will equal 0. As $|\delta|$ increases, and the input frequency is further detuned from $N\omega_{\rm out}$, ϕ goes to the first or fourth quadrant [see (25)]. As an example, Fig. 12 shows the phase portrait of the circuitry around the stable point at different values of n for $Q = 13$ and $V_{\rm in} = 0.695$ mV. Since in first and fourth quadrants, $\cos(2\phi) > 0$, consequently, $\lambda_2 < 0$. Thus, to find the locking range in this case, we only need to find the condition where λ_1 stays negative. In this case, the locking range equals

$$\frac{\delta_{\rm Lock}}{2}\omega_{\rm out} = \pm\frac{I_s I_1(\alpha)}{4CV_T}\sqrt{1 - \left(\frac{2RC}{L}\cdot\frac{V_T}{I_s I_1(\alpha)} - \frac{I_0(\alpha)}{I_1(\alpha)}\right)^2} \tag{27}$$

when $I_0(\alpha) < (2RC/L).(V_T/I_s)$. Thus, in this case, by detuning more than $\delta_{\rm Lock}$ derived in (27), the startup condition will not be satisfied and oscillation will be stopped.

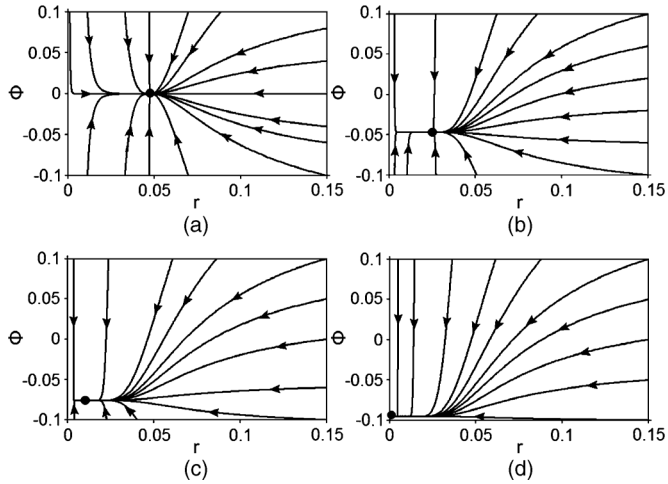


Fig. 12. Phase portrait of the circuitry around the stable point at different values of n: (a) $n = 2$, (b) $n = 1.97$, (c) $n = 1.95$, and (d) $n = 1.93$ for $Q = 13$ and $V_{\rm in} = 0.695$ mV.

For the other fixed point, we have $\sin(2\phi) = \pm 1$ at the edge of locking; thus, $\cos(2\phi) = 0$ and $\cos(4\phi) = -1$. Therefore, the second fixed point is

$$r^2 = 4(2V_T)^3\frac{\dfrac{-RC}{L} + \dfrac{I_s I_0(\alpha)}{2V_T}}{I_s\left[3I_0(\alpha) - I_2(\alpha)\right]}$$
$$\frac{\delta}{2}\omega_{\rm out} = -\frac{I_s I_1(\alpha)}{4CV_T}\left[1 - \left(\frac{r}{2V_T}\right)^2\right] \tag{28}$$

corresponding to asynchronous oscillations [see Fig. 11(b)]. Thus, the locking range equals

$$\frac{\delta_{\rm Lock}}{2}\omega_{\rm out} = \pm\left\{\frac{-I_s I_1(\alpha)}{4CV_T} + I_1(\alpha)\frac{\dfrac{-2R}{L} + \dfrac{I_s I_0(\alpha)}{CV_T}}{3I_0(\alpha) - I_2(\alpha)}\right\}. \tag{29}$$

In this case, by detuning more than $\delta_{\rm Lock}$ derived in (29), the oscillator goes out of locking range and it shows asynchronous oscillation. As mentioned above, at the edge of these two regions, we have

$$I_0(\alpha) = \frac{2RC}{L}\times\frac{V_T}{I_s}. \tag{30}$$

Fig. 13 shows the input power at the edge of the oscillation dying and pulling versus Q. For this calculation, maximum α is derived from (30) and then replaced in (22) to find $P_{\rm in,max}$. Fig. 14(a) shows the locking range versus the input power for $Q = 13$ and 6. The calculation uses (27) and (29) for each region. Since the model in not valid when the output voltage saturates, (29) cannot predict the locking range accurately in that case. Fig. 14(b) shows the locking range versus the input power for two different tank capacitance C, while $f_{\rm in} = 2f_{\rm out} = 5.29$ MHz and $Q = 13$. Since lower capacitance requires lower power for oscillation, it provides higher locking range with smaller input power.

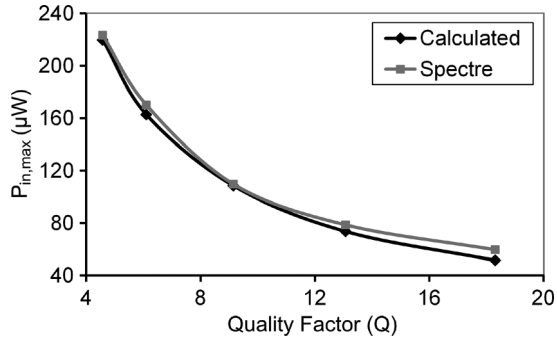


Fig. 13. Input power at the edge of oscillation dying and pulling versus tank quality factor (Q).

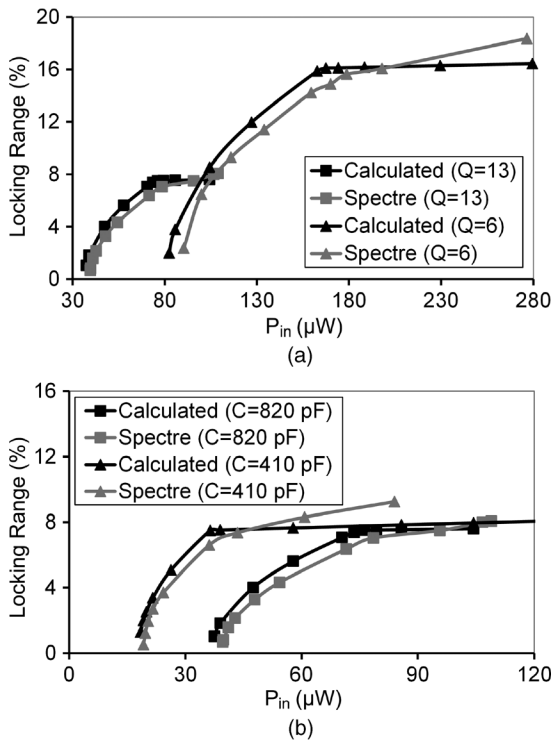


Fig. 14. Locking (tuning) range versus input power at $N = 2$ for: (a) $Q = 13$ and 6 and (b) $C = 820$ pF and 410 pF.

Following the same above-mentioned procedure, the locking range for $N = 1$ in the two regions equals

$$\delta_{\text{Lock}}\omega_{\text{out}} = \pm \frac{I_s I_2(\alpha)}{4CV_T}\sqrt{1-\left(\frac{2RC}{L}\cdot\frac{V_T}{I_s I_2(\alpha)}-\frac{I_0(\alpha)}{I_2(\alpha)}\right)^2}$$

$$\delta_{\text{Lock}}\omega_{\text{out}} = \pm\left\{\frac{-I_s I_2(\alpha)}{4CV_T}+I_2(\alpha)\frac{\dfrac{-2R}{L}+\dfrac{I_s I_0(\alpha)}{CV_T}}{3I_0(\alpha)-I_4(\alpha)}\right\}. \quad (31)$$

For $N = 4$, *only* oscillation pulling happens by detuning n. The reason is that $\dot{\phi} = 0$ for $r = 0$. Therefore, the locking range limited by the oscillation pulling is

$$\frac{\delta_{\text{Lock}}}{4}\omega_{\text{out}} = \pm\frac{I_1(\alpha)}{3I_0(\alpha)}\left[\frac{-R}{2L}+\frac{I_s I_0(\alpha)}{4CV_T}\right]. \quad (32)$$

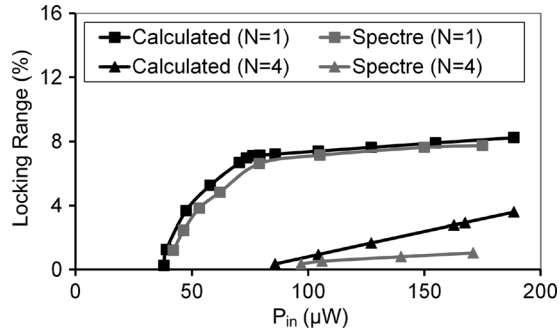


Fig. 15. Locking (tuning) range versus input power at $N = 1$ and $N = 4$ for $Q = 13$.

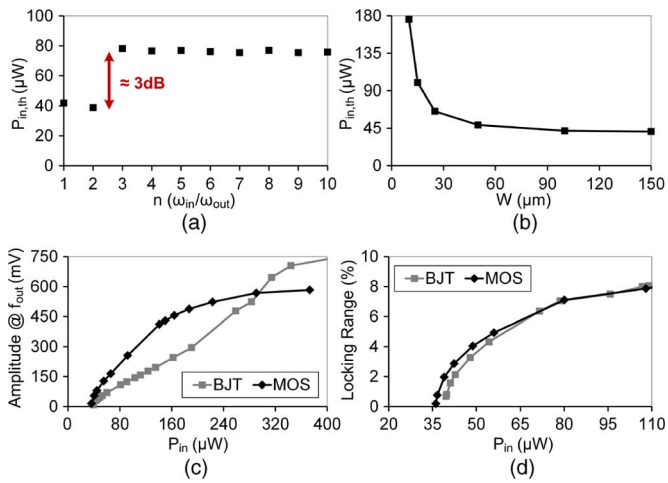


Fig. 16. Simulated minimum required input power for startup $P_{\text{in,th}}$ versus: (a) $n = \omega_{\text{in}}/\omega_{\text{out}}$ and (b) nMOS channel width W at $n = 2$; (c) the steady-state amplitudes r_{ss}, and (d) locking (tuning) range versus P_{in} at $n = 2$ and $Q = 13$.

Fig. 15 shows the locking range versus the input power for $N = 1$ and $N = 4$ when $Q = 13$. For $N = 3$ and $N \geq 5$, since $\dot{\phi} = 0$, detuning does not have any effect on the oscillation frequency. Therefore, the circuit will show an asynchronous oscillation and the output signal cannot lock to the input signal (basically the locking range is zero).

E. MOSFET Nonlinear Core

In Sections III-A–III-D, the nonlinear core is assumed to consist of BJT transistors. The exponential *I–V* characteristic of BJT eases the analysis and enables derivation of closed-form expressions from which intuition can be gained. In this section, we briefly discuss the effect of using MOSFET transistors in the nonlinear core. The *I–V* characteristic of MOS transistors is not as well behaved, especially as transistor enters different operation regions (e.g., saturation, triode) throughout the large-signal operation. However, based on the simulation results, the circuit function does not depend on the exact nonlinear function. The simulations are done for the same schematic shown in Fig. 3(a), except that the BJT transistors are replaced with nMOS transistors in a 0.13-μm CMOS technology. The same passive devices have been used ($L = 2.2$ μH, $C = 820$ pF, $R = 2.8$ Ω, corresponding to a tuned frequency of approximately 2.64 MHz and Q of 13 at 2.64 MHz). Fig. 16(a) shows the minimum required

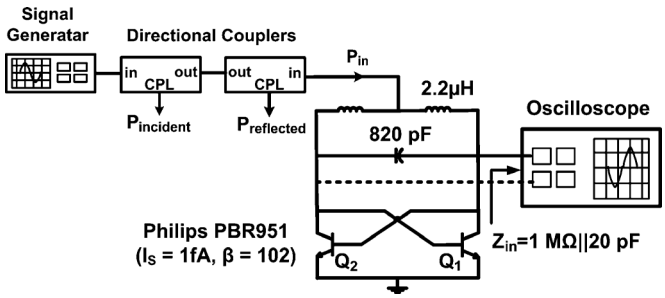


Fig. 17. Measurement setup for the low-frequency prototype.

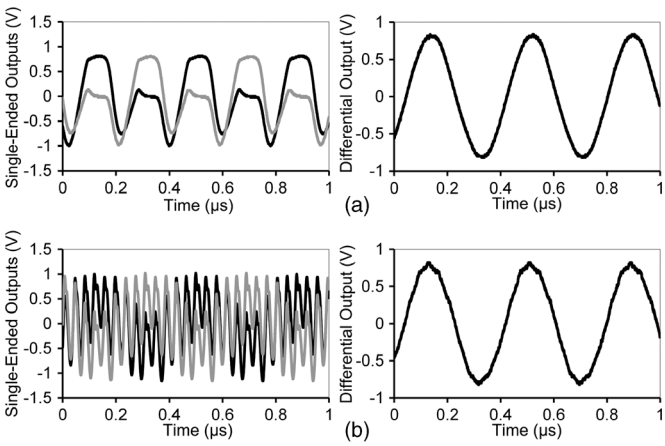


Fig. 18. Measured single-ended and differential output waveforms when: (a) $f_{\rm in} = 2f_{\rm out}$ and (b) $f_{\rm in} = 10f_{\rm out}$.

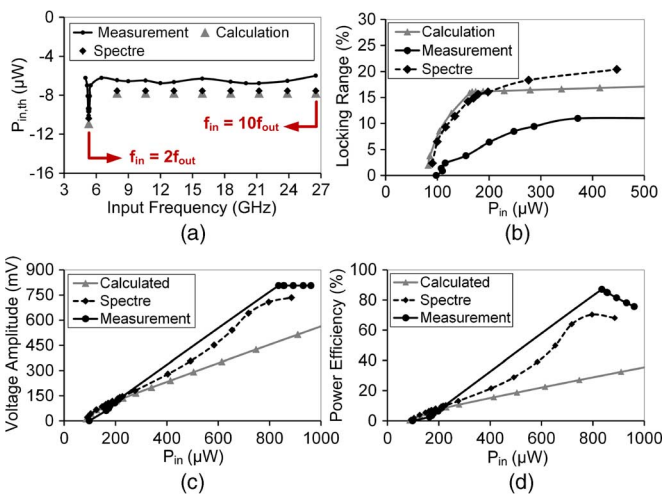


Fig. 19. Measured, simulated, and calculated: (a) minimum required input power ($P_{\rm in,th}$) for subharmonic generation versus the input frequency, (b) locking (tuning) range, (c) output amplitude, and (d) power efficiency versus input power at $n = 2$.

input power for the startup ($P_{\rm in,th}$) versus n with nMOS size of W/L $= 150\ \mu$m/130 nm. Similar to the case where BJT devices have been used, $n = 2$ requires the minimum input power and as n increases, $P_{\rm in,th}$ is relatively constant and approximately 3 dB more than $n = 2$. Fig. 16(b) shows $P_{\rm in,th}$ versus the width of the MOS transistor W when channel length

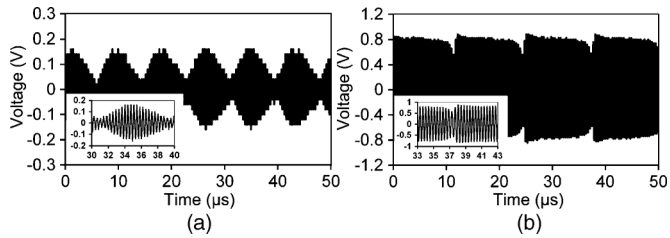
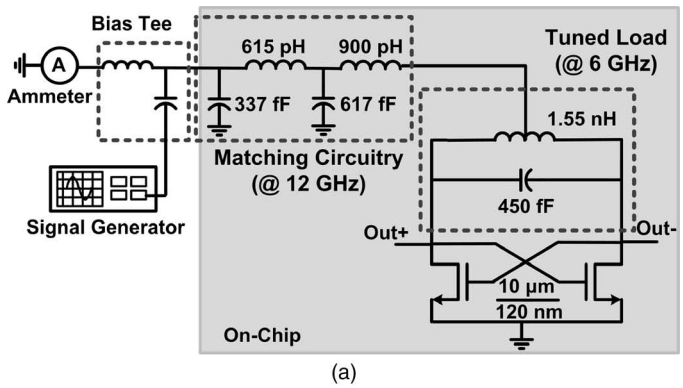


Fig. 20. Measured output waveforms when the downconverter is pulled for $n = 2$ at: (a) $P_{\rm in1}$ and (b) $P_{\rm in2}$, where $P_{\rm in1} < P_{\rm in2}$. Zoomed versions are shown in the respective insets.



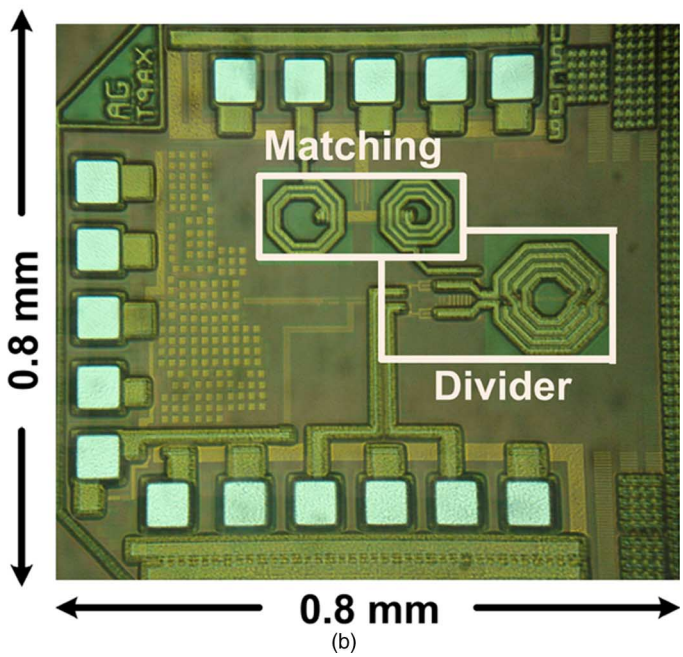


Fig. 21. (a) Detailed schematic and (b) chip microphotograph of the integrated 12-GHz divide-by-2 self-powered divider.

is $L = 130$ nm and $n = 2$. Again, we see that larger transistors and smaller threshold voltages are beneficial as they reduce the minimum input power requirement. $P_{\rm in,th}$ also shows stronger dependence on the device size at small device sizes. Fig. 16(c) shows the steady-state amplitude $r_{\rm ss}$ versus $P_{\rm in}$, when $W/L = 150\ \mu$m/130 nm for $n = 2$ in comparison with the BJT case.[1] Fig. 16(d) shows the locking range versus the input power, which is very close in both the BJT and CMOS cases.

[1]The circuitry with this size of nMOS transistor requires the same $P_{\rm in,th}$ as a circuitry using a BJT with $I_s = 0.963$ fA.

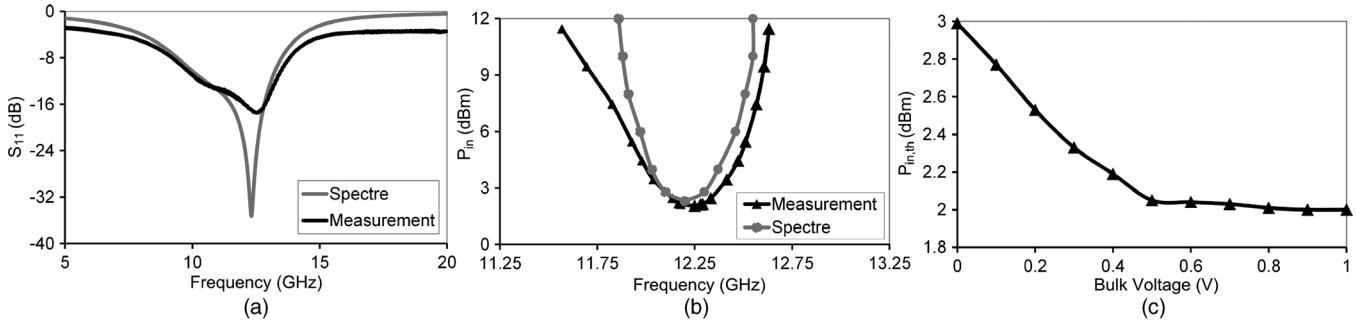


Fig. 22. Measured and simulated: (a) S_{11} (return loss), (b) sensitivity curve, and (c) measured $P_{\mathrm{in,th}}$ versus the transistor bulk voltage.

IV. Implementation and Measurement Results

In this section, measurements results for discrete and integrated prototypes verifying the analytical claims are presented.

A. Discrete Frequency Downconverter

To experimentally demonstrate the generation of various subharmonic signals in the synchronous operation mode and verify the corresponding locking ranges, the configuration shown in Fig. 2 is implemented. The BJTs and passives are the same used in calculations and simulations (the BJT transistor is PBR951, $L = 2.2$ μH, and $C = 820$ pF). The measurement setup is depicted in Fig. 17. For the measurements, a high input-impedance oscilloscope (Tektronix TDS2024C) has been used; therefore, no output buffer was required. Since there is no matching circuitry at the input, directional couplers have also been used to extract the value of the input power that goes into the circuitry.

Representative measured single-ended and differential output waveforms of the circuit for $f_{\mathrm{in}} = 2f_{\mathrm{out}}$ and $f_{\mathrm{in}} = 10f_{\mathrm{out}}$ are shown in Fig. 18(a) and (b), respectively. As expected, each single-ended signal has both the input frequency ω_{in} and output frequency ω_{out} components. Fig. 19(a) shows the measured, simulated, and calculated minimum required input power $(P_{\mathrm{in,th}})$ for subharmonic generation (not necessarily synchronous) versus the input frequency. As expected, dividing by 2 $(n = 2)$ requires the minimum input power, and as frequency increases, almost a constant input power is required. As predicted before, the difference in $P_{\mathrm{in,th}}$ for $n = 2$ and $n > 2$ is about 3 dB. The measured, simulated, and calculated locking range for $n = 2$ versus the input power is depicted in Fig. 19(b). The differential output amplitude and power efficiency are shown in Fig. 19(c) and (d), respectively. A Q of 6 is assumed for the simulation and calculation to match to the measurement results. As an example, the measured differential output voltages during the circuit pulling at two different input power levels for $n = 2$ are also shown in Fig. 20.

B. Integrated 12-GHz Divide-by-2 Self-Powered Divider

As shown before, division-by-2 requires lowest input power and also provides highest efficiency. In order to demonstrate the applicability of this technique at higher frequencies, an integrated 12-GHz divide-by-2 circuitry is designed and fabricated in a 0.13-μm CMOS technology with eight metal layers (Fig. 21). As mentioned in Section IV-A, smaller threshold voltage for the switching pair transistors relaxes the startup condition; therefore, triple-well transistors have been used with positive bulk voltage to reduce the threshold voltage. The bulk and N-well of the transistors have also been floated with a large resistance (1.1 MΩ) to reduce the parasitic capacitance. The input at 12 GHz is matched to 50 Ω using the $L_1C_1L_2C_2$ ladder network. From simulations, the loss of the matching circuitry network at 12 GHz is about 2 dB, while the Q of the resonance tank at 6 GHz is approximately 15. An open-drain output buffer has been placed after the divider to facilitate measurements.

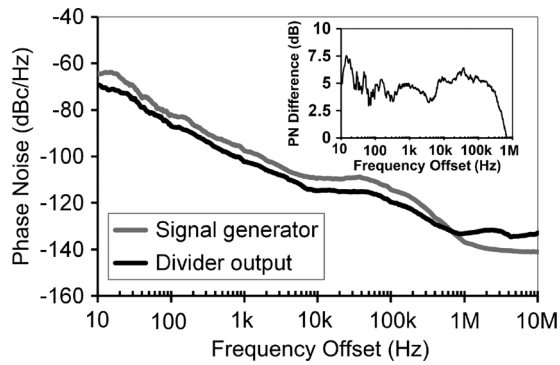


Fig. 23. Measured phase noise of the signal generator and the 12-GHz divider output.

The N-well and bulk voltages are kept at 1.5 and 0.5 V, respectively. Fig. 22(a) shows the small-signal input reflection coefficient S_{11} when $P_{\mathrm{in}} = -7$ dBm. The measured and simulated sensitivity curves (locking range) are shown in Fig. 22(b); the minimum required input power is about 2 dBm, while the locking range is approximately 1 GHz at $P_{\mathrm{in}} = 11.45$ dBm. Fig. 22(c) shows the measured $P_{\mathrm{in,th}}$ versus the bulk voltage. As the bulk voltage increases, the threshold voltage of the nMOS transistors reduces; thus the input power for startup also reduces. Fig. 23 shows the measured phase noise of the signal generator (Agilent E8257C) and the 12-GHz divider output. Table I summarizes the performance of this 12-GHz divider in comparison with other recent reported passive and active dividers.

C. Effect of a DC Block on the Divider Performance

The simulated single-ended voltage and transistor current waveforms in the 12-GHz divider are shown in Fig. 24(a). The current waveform is asymmetric with respect to time so it has a dc component. This dc current helps the circuitry to satisfy the startup condition easier since smaller ac current (and therefore,

TABLE I
PERFORMANCE COMPARISON AMONG DIFFERENT PASSIVE AND ACTIVE DIVIDERS

Ref.	Frequency (GHz)	VDD (V)	P_{DC} (mW)	$P_{in,th}$(dBm) /$V_{in,th}$(V)	Locking Range	Topology	Area (mm²)	Technology
[11]	2	3	N/A	-14 dBm	0.4 GHz @ 0 dBm	Active Parametric	-	Discrete pHEMT
[14]	20	0	0	440 mV	1 GHz @ 0.6 V	Passive Parametric	0.75 x 0.32 (Active)	0.13 μm CMOS
[22]	7	0.8	0.9	-28 dBm	2.43 GHz @ 0 dBm	Injection-Locked	0.22 x 0.15 (Active)	0.13 μm CMOS
[23]	23.5	0.9	8.28	-30 dBm	3.2 GHz @ 0 dBm	Injection-Locked	0.74 x 0.84	0.18 μm CMOS
[24]	21.35	0.8	1.51	-12 dBm	4.1 GHz @ 10 dBm	Injection-Locked	0.23 (Active)	0.13 μm CMOS
This Work	**12**	**0**	**0**	**2 dBm (with matching)**	**1 GHz @ 11.45 dBm**	**Memoryless Nonlinearity**	**0.8 x 0.8**	**0.13 μm CMOS**

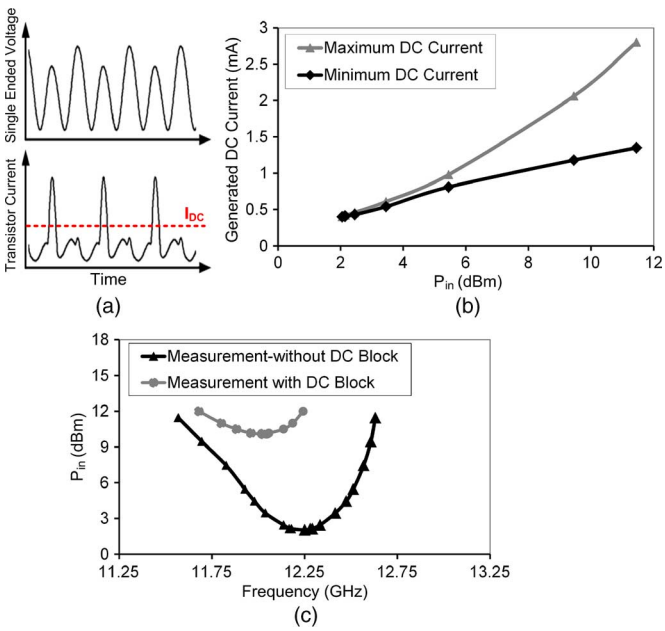


Fig. 24. (a) Simulated single-ended voltage and transistor current waveforms. (b) Measured maximum/minimum generated dc current in the 12-GHz divider. (c) Measured sensitivity curve with/without dc block at the input.

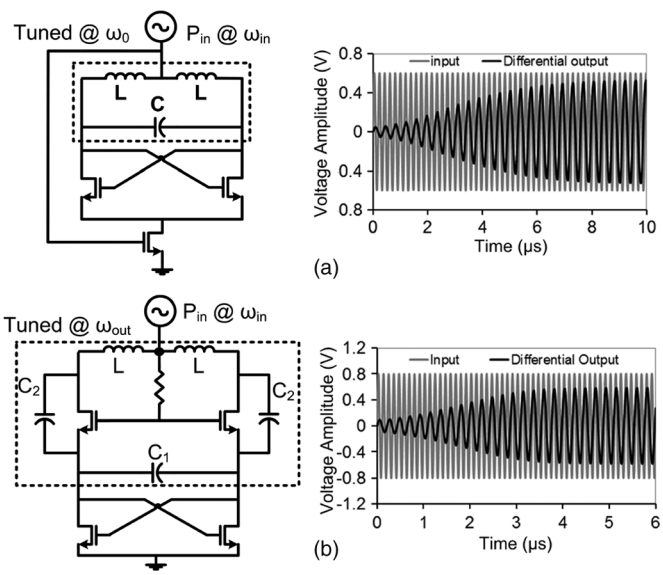


Fig. 25. Alternative configuration for the proposed passive subharmonic generator without any dc power supply and their representative inpu/output waveforms. (a) Differential cross-coupled oscillator with tail transistor ($f_{\rm in} = 2f_{\rm out} = 5.29$ MHz). (b) Differential noise-shifting Colpitts oscillator ($f_{\rm in} = 2f_{\rm out} = 9$ MHz) [25].

smaller $P_{\rm in}$) will be required for oscillation. The presence of the dc current in the system equations has also been shown in the previous sections ($I_0(\alpha)$). Fig. 24(b) shows the measured maximum and minimum generated dc current in the 12-GHz divider. However, the functionality of the frequency divider does not depend on the existence of the dc current in the circuit. To prove this, a dc block is placed in series with the input (the dc port of the bias-tee is floated now). Fig. 24(c) shows the measured sensitivity curve before and after using the dc block. The circuit functions with and without dc current. However, the performance of the circuit degrades significantly when the dc current is blocked. Strangely, in the case of low-frequency discrete prototype, the circuit does not function when the dc current is blocked. This is against our expectation and still not understood.

V. CONCLUSIONS AND DISCUSSIONS

This paper presents a passive frequency downconverter to transfer energy from a higher frequency source to a lower frequency, which can be a subharmonic of the input source, without consuming dc power. In the proposed technique, a memoryless nonlinear core coupled to a linear passive resonator is exploited for frequency downconversion. While all analysis, designs, and experimental results correspond to the cross-coupled differential pair active core, the principles are general and applicable to other similar circuits as well. Fig. 25 shows the proposed batteryless passive subharmonic frequency generation scheme with alternative nonlinear cores, along with their representative simulated input/output waveforms.

The major motivation for this study is to enable batteryless systems that must extract energy from electromagnetic

emissions. Extracting power from higher RF frequencies is advantageous from the antenna size standpoint. However, the main challenge with high-frequency power harvesting is the low RF-to-dc power conversion efficiency of most rectifiers. For example, a reported millimeter-wave power harvesting system shows the RF-to-dc conversion efficiency of around 1.2% for the rectifier at 45 GHz, including the losses of the on-chip matching network [26]. Efficient batteryless subharmonic generation followed with an efficient low-frequency rectifier may result in a more efficient solution for high-frequency power harvesting.

APPENDIX A

In this appendix, detailed analysis to find the startup condition for the $n = 2$ case is presented. First, the fixed points or the solutions to the simplified averaged differential equations [see (16)] are found. In order to analyze the stability of these solutions, the eigenvalues of the Jacobean matrix [see (33)] should be evaluated at each fixed point

$$\begin{bmatrix} \frac{\partial \dot{\bar{r}}}{\partial r} & \frac{\partial \dot{\bar{r}}}{\partial \phi} \\ \frac{\partial \dot{\bar{\phi}}}{\partial r} & \frac{\partial \dot{\bar{\phi}}}{\partial \phi} \end{bmatrix}. \tag{33}$$

The nonzero fixed points are

$$\begin{aligned} [r^2, \phi] &= \left[0, \frac{k\pi}{2}\right] \\ [r^2, \phi] &= \left[(2V_T)^3 \frac{\frac{-R}{2L} + \frac{I_s}{4CV_T}\left[I_0(\alpha) + I_1(\alpha)\right]}{\frac{I_s}{2C}\left[\frac{3}{4}I_0(\alpha) + I_1(\alpha) + \frac{1}{4}I_2(\alpha)\right]}, k\pi\right] \\ [r^2, \phi] &= \left[(2V_T)^3 \frac{\frac{-R}{2L} + \frac{I_s}{4CV_T}\left[I_0(\alpha) - I_1(\alpha)\right]}{\frac{I_s}{2C}\left[\frac{3}{4}I_0(\alpha) - I_1(\alpha) + \frac{1}{4}I_2(\alpha)\right]}, \right. \\ &\qquad \left. (2k+1)\frac{\pi}{2}\right]. \end{aligned} \tag{34}$$

The first solution, $r = 0$, $\cos(2\phi) = \pm 1$, has the following eigenvalues:

$$\begin{aligned} \lambda_1 &= \frac{-R}{2L} + \frac{I_s}{4CV_T}\left[I_0(\alpha) + I_1(\alpha)\cos(2\phi)\right] \\ \lambda_2 &= \frac{-I_s I_1(\alpha)}{2CV_T}\cos(2\phi). \end{aligned} \tag{35}$$

Therefore, $r = 0$, and $\cos(2\phi) = -1$ is either a saddle point or an unstable point, depending on the value of α. However, $r = 0$, $\cos(2\phi) = 1$ will be a saddle point if $(-R/2L) + (I_s/4CV_T)[I_0(\alpha) + I_1(\alpha)] < 0$ (which provides the startup condition); otherwise, it is a stable point. This is when the startup condition is not satisfied.

The second solution in (34) exists only when $(-R/2L) + (I_s/4CV_T)[I_0(\alpha) + I_1(\alpha)] > 0$, in which case both of the following eigenvalues will be negative:

$$\begin{aligned} \lambda_1 &= -2\left[\frac{-R}{2L} + \frac{I_s}{4CV_T}\left[I_0(\alpha) + I_1(\alpha)\right]\right] \\ \lambda_2 &= \frac{-I_s}{2CV_T}\left[I_1(\alpha) - V_T\left(I_1(\alpha) + I_2(\alpha)\right)\right. \\ &\qquad \left. \times \frac{\frac{-R}{2L} + \frac{I_s}{4CV_T}\left[I_0(\alpha) + I_1(\alpha)\right]}{\frac{I_s}{2C}\left[\frac{3}{4}I_0(\alpha) + I_1(\alpha) + \frac{1}{4}I_2(\alpha)\right]}\right]. \end{aligned} \tag{36}$$

Consequently, this will be a *stable* steady-state solution when $(-R/2L) + (I_s/4CV_T)[I_0(\alpha) + I_1(\alpha)] > 0$. The eigenvalues corresponding to the third solution in (34) are

$$\begin{aligned} \lambda_1 &= -2\left[\frac{-R}{2L} + \frac{I_s}{4CV_T}\left[I_0(\alpha) - I_1(\alpha)\right]\right] \\ \lambda_2 &= \frac{I_s}{2CV_T}\left[I_1(\alpha) - V_T\left(I_1(\alpha) - I_2(\alpha)\right)\right. \\ &\qquad \left. \times \frac{\frac{-R}{2L} + \frac{I_s}{4CV_T}\left[I_0(\alpha) - I_1(\alpha)\right]}{\frac{I_s}{2C}\left[\frac{3}{4}I_0(\alpha) - I_1(\alpha) + \frac{1}{4}I_2(\alpha)\right]}\right] \end{aligned} \tag{37}$$

which corresponds to a saddle point if $(-R/2L) + (I_s/4CV_T)[I_0(\alpha) - I_1(\alpha)] > 0$ and to an unstable point otherwise.

Therefore, if $(-R/2L) + (I_s/4CV_T)[I_0(\alpha) + I_1(\alpha)] > 0$, the second fixed point is the stable solution, satisfying the startup condition; otherwise, $r = 0$ becomes the stable point. It should be mentioned that the above fixed points are valid for small values of amplitude, due to the approximation in the $\tanh(x) \approx x - x^3/3$ function, which is suitable for the startup condition.

REFERENCES

[1] H. Q. North, "Properties of welded contact germanium rectifiers," *J. Appl. Phys.*, vol. 17, no. 11, pp. 912–923, Nov. 1946.

[2] J. M. Manley and H. E. Rowe, "Some general properties of nonlinear elements—Part I: General energy relations," *Proc. IRE*, vol. 44, no. 7, pp. 904–913, Jul. 1956.

[3] J. Hilibrand, C. W. Mueller, C. F. Stocker, and R. D. Gold, "Semiconductor parametric diodes in microwave computers," *IRE Trans. Electron. Comput.*, vol. EC-8, no. 3, pp. 287–297, 1959.

[4] R. G. Harrison, "A broadband frequency divider using microwave varactors," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-25, no. 12, pp. 1055–1059, Dec. 1977.

[5] Z. Nativ, "The application of a frequency multiplier design method to the design of microwave parametric dividers," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-35, no. 2, pp. 189–194, Feb. 1987.

[6] G. A. Kalivas and R. G. Harrison, "A new slotline-microstrip frequency halver," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 1985, pp. 683–686.

[7] R. G. Harrison and W. D. Cornish, "Varactor frequency halver with enhanced bandwidth and dynamic range," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 1986, pp. 305–308.

[8] S. P. Stapleton and M. G. Stubbs, "A microwave frequency halver with conversion gain," in *Eur. Microw. Conf. Dig.*, 1986, pp. 749–753.

[9] G. R. Sloan, "The modeling, analysis, and design of filter-based parametric frequency dividers," *IEEE Trans. Microw. Theory Techn.*, vol. 41, no. 2, pp. 224–228, Feb. 1993.

[10] A. Suárez and R. Melville, "Simulation-assisted design and analysis of varactor-based frequency multipliers and dividers," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 3, pp. 1166–1179, Mar. 2006.

[11] Z. Heshmati, I. C. Hunter, and R. D. Pollard, "Microwave parametric frequency dividers with conversion gain," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 10, pp. 2059–2064, Oct. 2007.
[12] Z. Zhao, J. Bousquet, and S. Magierowski, "Coherent parametric RF downconversion in CMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2010, pp. 377–380.
[13] S. Magierowski, J. Bousquet, Z. Zhao, and T. Zourntos, "RF CMOS parametric downconverters," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 3, pp. 518–528, Mar. 2010.
[14] W. Lee and E. Afshari, "Distributed parametric resonator: A passive CMOS frequency divider," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1834–1844, Sep. 2010.
[15] M. Luukkala, "Fine structure of fractional harmonic phonons," *Phys. Lett. A*, vol. 25, no. 2, pp. 76–77, Jul. 1967.
[16] M. Luukkala, "Threshold and oscillation of fractional phonons," *Phys. Lett. A*, vol. 25, no. 3, pp. 197–198, Aug. 1967.
[17] H. Mahon, E. Brun, M. Luukkala, and W. G. Proctor, "Excitation of fractional harmonic phonons in solids," *Phys. Rev. Lett.*, vol. 19, no. 8, pp. 430–432, 1967.
[18] P. J. King and M. Luukkala, "Subharmonic generation in quartz plates," *J. Phys. D, Appl. Phys.*, vol. 6, pp. 1047–1051, 1973.
[19] Z. Safarian and H. Hashemi, "Passive subharmonic generation using *LC*-oscillators," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2012, pp. 1–3.
[20] M. Abramowitz and I. A. Stegun, *Handbook of Mathematical Functions With Formulas, Graphs and Mathematical Tables*, 9th ed. New York: Dover, 1972, pp. 358–364.
[21] N. Kryloff and N. Bogoliuboff, *Introduction to Nonlinear Mechanics*. Princeton, NJ: Princeton Univ. Press, 1947.
[22] R. Sujiang, A. W. L. Ng, and H. C. Luong, "0.9 mW 7 GHz and 1.6 mW 60 GHz frequency dividers with locking-range enhancement in 0.13 μm CMOS," in *Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2009, pp. 96–97.
[23] Y. Chen, M. Li, H. Kuo, T. Huang, and H. Chuang, "Low-voltage K-band divide-by-3 injection-locked frequency divider with floating-source differential injector," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 1, pp. 60–67, Jan. 2012.
[24] Z. Huang, C. Wu, and B. Huang, "Design of 24-GHz 0.8-V 1.51-mW coupling current-mode injection-locked frequency divider with wide locking range," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 8, pp. 1948–1958, Aug. 2009.
[25] R. Aparicio and A. Hajimiri, "A noise-shifting differential Colpitts VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1728–1736, Dec. 2002.
[26] S. Pellerano, J. Alvarado, and Y. Palaskas, "A mm-wave power-harvesting RFID tag in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1627–1637, Aug. 2010.

Zahra Safarian (S'12) received the B.Sc. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 2005, the M.S. degree in electrical engineering from the University of Southern California (USC), Los Angeles, in 2008, and is currently working toward the Ph.D. degree at USC.

The focus of her current research is the design of low-power integrated systems for biomedical applications.

Hossein Hashemi (S'99–M'03–SM'08) received the B.S. and M.S. degrees in electronics engineering from the Sharif University of Technology, Tehran, Iran, in 1997 and 1999, respectively, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, in 2001 and 2003, respectively.

In 2003, he joined the Ming Hsieh Department of Electrical Engineering Electrophysics, University of Southern California (USC), Los Angeles, where he is currently an Associate Professor, Ming Hsieh Faculty Fellow, and Co-Director of the Ming Hsieh Institute. His research interest spans mathematics, physics, and realization of integrated electrical and optical systems.

Dr. Hashemi currently serves on the Technical Program Committees of the IEEE International Solid-State Circuits Conference (ISSCC), the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, and the Compound Semiconductor Integrated Circuits Symposium (CSICS). He was an associate editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS (2006–2007) and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS (2004–2005). He was the recipient of the 2008 Defense Advanced Research Projects Agency (DARPA) Young Faculty Award, the National Science Foundation (NSF) CAREER Award, and the USC Viterbi School of Engineering Junior Faculty Research Award (2008). He was recognized as a Distinguished Scholar for the Outstanding Achievement in Advancement of Engineering by the Association of Professors and Scholars of Iranian Heritage (2011). He was a corecipient of the 2004 IEEE JOURNAL OF SOLID-STATE CIRCUITS Best Paper Award and the 2007 IEEE International Solid-State Circuits Conference (ISSCC) Lewis Winner Award for Outstanding Paper.