Abstract: The massive explosion in data acquisition, processing, and archiving, hindered by the end of Moore’s Law, creates an opportunity for a complete redesign of the information technology stack, including hardware system architectures, devices, networks, and software to enable future computing systems with multi-exascale performance—and beyond. Key to success in this challenging endeavor will be the paradigm shift of moving from a processor-centric to a memory-centric approach. Architectural changes are necessary to overcome the limitations of the traditional compute-centric model, and will require new network layouts (e.g., Hyper-X) and new high-performance memory-addressing protocols (e.g., Gen-Z) that rely on a high-bandwidth and energy-efficient photonic interconnect. We will describe the state-of-the-art in datacom photonics and present the advances that will be necessary—and are already appearing in R&D laboratories—to enable memory-centric computing at scale.

Memory-centric computing would be an ideal heterogeneous platform for in-memory hardware accelerators that can be brought to bear on specific problems of scientific, engineering, or industrial interest. Ideally, a mature software ecosystem would simplify the design of a plug-and-play network interface that would allow users to compare the performance of the most advanced accelerators. We will describe such an accelerator—a coherent optical Ising machine—that targets NP-hard problems that scale exponentially as a function of system size and are common to applications such as traffic flow optimization, supply chain management, airline scheduling, and DNA sequencing. Optical Ising machines based on symmetry-breaking in pulsed optical parametric oscillators have already been shown to outperform a commercially-available quantum annealer, and there is good reason to believe that integrated photonic implementations of this approach can achieve similar results.