Gourav Datta

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EDUCATION

- **University of Southern California** — Los Angeles, CA
  PhD in Electrical Engineering with focus on VLSI Design; Major GPA: 4/4; advisor: Dr. Peter Beerel — *August 2018 – present*
  Major courses taken: Design for Testability, Computer Systems Organization, Advanced Computer Architecture, Analysis of Algorithms, VLSI System Design, Probability and Statistics, Machine Learning, Deep Learning.
- **Indian Institute of Technology** — Kharagpur, India
  B.Tech in Instrumentation Engineering (minor in Electronics); GPA: 9.00 /10.0 (Class Rank-1) — *August 2014 – May 2018*
  Graduate courses taken: Architectural Design of IC, VLSI CAD, Computer Architecture, Semiconductor Devices

SELECTED EXPERIENCE

- **Stealth Startup, Senior Research Engineering Internship** — Portland, OR
  ***Logic Design using Ferroelectrics**; Manager: Dr. Sasikanth Manipatruni* — *May 2020 - August 2020*
  - Developed a new class of ferroelectric logic based on low voltages, high charge density and non-volatility to power the next generation of computing with a 100x improvement in energy efficiency compared to CMOS Boolean logic.
- **Apple Inc., CPU Design Implementation Team (Summer Internship)** — Cupertino, CA
  ***Logic Synthesis for Timing**; Manager: Shashank Shastry* — *May 2019 - August 2019*
  - **Synthesis**: Explored *synthesis techniques* to improve timing of a design given its' RTL and used design metrics like WNS, TNS, etc. to evaluate their benefit.
    - *Functionally efficient cell usage*, which can improve placement and routing, thereby improving TNS.
    - *Fanout optimization using flop and logic duplication* with the expectation that WNS improves without impacting density and power.
  - **Timing closure**: Worked closely with the methodology and the CAD team to implement the above techniques and come up with new recipes to close setup and hold timing violations.
- **University of Southern California (Graduate Research)** — Los Angeles, CA
  Rethinking the whole Computing stack (Circuit-Architecture-Algorithm Co-Simulation) — *Aug. 2018 - Present*

  Synchronization and Computational units for Single Flux Quantum (SFQ) technologies
  - Designed an efficient gate level pipelined 32-bit ALU for SFQ processors. Parallel 4-bit Sklanskey adder blocks are used as building blocks in a block-skewed manner to improve throughput for data dependent operations.
  - Designed a metastability-resilient clock domain crossing FIFO synchronizer (inspired by CMOS 2-flop synchronizers) that simulations show delivers 1000 reduction in logical error rate at 30 GHz compared to state-of-the-art designs.

  Design of a Superconducting L_1 Cache Memory
  - Developed a novel direct-mapped SFQ Cache that promises higher throughput than the state-of-the-art based on circular FIFOs. Our design enables direct access to memory cells and split and merge elements to reduce overhead.
  - Completed JSIM models to compare the JJ complexity and feasible performance to the baseline. Initial analysis shows the potential for significant increase in performance and power with a reasonable increases in JJ complexity.

  Algorithm-hardware co-design for In-pixel Analog Computing for Computer Vision applications
  - Designed novel algorithms and customized architectures for lightweight neural networks targeting end applications that can be accelerated by non-volatile memory (NVM) based in-pixel sensor hardware.
  - Benchmarked power and performance for the system level implementation of the proposed in-pixel hardware.

  Hardware Acceleration of Bayesian Neural Networks (BNN) using Stochastic Memristors
  - Developed learning algorithms for BNNs to be implemented in memristive crossbar array based in-memory computing hardware that exploits the experimentally demonstrated cycle-to-cycle variability of the devices.

  Algorithm-hardware Co-design for Energy-efficient Event-driven Inference
  - Developed novel neuro-inspired learning algorithms tailored towards GPUs which can yield orders of magnitude improvement in energy-efficiency for image classification tasks compared to traditional deep neural networks.
  - Proposed a novel architecture that can process a set of input spikes using an output-stationary dataflow model, along with a hybrid on-chip memory to accelerate Spiking Neural Networks (SNN) workloads.
- **INRIA Research Centre (Research Internship)** — Rennes, France
  ***C-based Synthesis Modelling for RISC-V processor**; advisor: Dr. Olivier Sentieys* — *May 2017 - July 2017*
  - Designed an in-order core micro-architecture supporting 32-bit RISC-V instruction set from C-based specifications using High Level Synthesis(HLS) tools.
  - Validated the design with real time RISC-V benchmarks and synthesized the core down to gate level. Finally, compared simulation results(clock frequency, area, power) with some existing RISC-V designs, such as Rocket core.

SELECTED PUBLICATIONS

1. **G. Datta**, S. Kundu, H. Cong, P. A. Beerel, "qCDC: Metastability-Resilient Synchronization FIFO for SFQ Logic," *International Superconductive Electronics Conference (ISEC) 2019.*
2. S. Kundu, **G. Datta**, P.A. Beerel, M. Pedram, "qBSA: Logic Design of a 32-bit Block-Skewed RSFQ Arithmetic Logic Unit," *ISEC, 2019.*
3. A. Abdelhadi, D. Chen, H. Cheng, **G. Datta**, Y. Zhang, P. A. Beerel, M. Greenstreet, "Two-Phase Asynchronous to Synchronous Interfaces for an Open-Source Bundled-Data Flow," *International Symposium on Asynchronous Circuits and Systems (ASYNC) 2019.*
4. **G. Datta**, P.A. Beerel, "Modeling and Characterization of Metastability in Single Flux Quantum (SFQ) Synchronizers," *in International Symposium on Circuits and Systems (ISCAS) 2020.*
5. **G. Datta**, P.A. Beerel, "Single Flux Quantum (SFQ) First-in-first-out (FIFO) Synchronizers: New Designs and Paradigms," *in IEEE Transactions on Applied Superconductivity.*
6. **G. Datta**, P.A. Beerel, "Metastability in Superconducting Single Flux Quantum(SFQ) Logic," *accepted in IEEE Transactions on Circuits and Systems-I.*
7. S. Kundu, **G. Datta**, M. Pedram, P.A. Beerel, "Spike-Thrift: Towards Energy-Efficient Deep Spiking Neural Networks by Limiting Spiking Activity via Attention-Guided Compression," *accepted in Winter Conference on Applications of Computer Vision (WACV) 2020.*
8. **G. Datta**, Souvik Kundu, P.A. Beerel, "Training Energy-efficient Deep Spiking Neural Networks with Single-Spike Hybrid Input Encoding" *under review in International Joint Conference on Neural Networks (IJCNN), 2021.*
9. S. Kundu, **G. Datta**, M. Pedram, P.A. Beerel, "Towards Energy-Efficient Deep Spiking Neural Networks via Attention-Guided Compression," *under review in IEEE Transactions on Neural Networks and Learning Systems, 2021.*
10. **G. Datta**, S. Kundu, A.K. Jaiswal, P.A. Beerel, "Processing-in-Memory (PIM) Acceleration of Quantized Deep Spiking Neural Networks for Hyperspectral Image Classification," *to be submitted to IEEE Transactions on Neural Networks and Learning Systems, 2021.*

COURSE PROJECTS

- **Embedded System Design Mini Project**: Feb 2017 - Apr 2017
  - Acquied, amplified, filtered and displayed ECG signals using STM32F4 MCU and Altera Cyclone IV FPGA.
  - The FIR filter and UART transmitter/receiver is implemented on the FPGA. The FPGA applies FIR filtering to the signals and sends them back to the MCU.
- **VLSI Design Mini Project**: May 2016 - Jul 2016
  - Performed RTL design for Hamming distance based pattern matching(with and without parallelism) using IC compiler.
  - Designing an efficient general purpose Multi-Cycle CPU that supports arithmetic, logical and memory read/write operations. A 1024-bit SRAM is utiized as Data memory. Used python to read assembly code and generate vector file for control signals.
- **Design for Testability Mini Project**: Implemented an ATPG algorithm(PODEM) and a Deductive Fault Simulator for some ISCAS'85 bencmark circuits. Achieved high fault coverage(>99%) for all circuits. Sept 2018 - Present
- **Design of a low power analog correlator for neural spike sorting (B.Tech Project)**: Aug 2017 - May 2018
  - Designed an analog correlator for neural spike sorting, involving the use of switched capacitor circuits along with digital control. 6-T SRAM cells were designed to store the spike templates.
  - A low noise front end amplifier was integrated with the correlator to reduce the effect of background noise in spike sorting.

ACADEMIC ACHIEVEMENTS

- **USC Annenberg Fellowship:** Top few incoming Graduate students at USC.
- **Academic Excellence:** Adjudged the academically best outgoing student in the batch of Instrumentation Engineering at IIT Kharagpur. Also, received 2 additional academic excellence awards during the academic session 2017-2018.

TECHNICAL SKILLS

- **Programming Languages**: C, C++, Python. **Simulation Environments**: Cadence Virtuoso, Synopsis (PnR Tool), Catapult HLS, MATLAB, Modelsim, Xilinx ISE. **HDLs**: Verilog, System-verilog. **ML Tools**: Pytorch, Tensorflow

VOLUNTARY EXPERIENCE

- **Teaching Assistant** at IIT Kharagpur for two undergraduate courses, Signals and Networks and Analog Electronics during the Academic Session 2016 - 2017.
- **Student mentor** of Student Welfare Group of IIT Kharagpur, having mentored 5 undergraduate students in their academic courses.

Last updated: April 8, 2021.