**Mostafa A. Abouelkassem**  
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**EDUCATION**

**The University of Southern California, Viterbi School of Engineering,** Los Angeles, CA

**Ph.D.**, Electrical Engineering. **GPA 4/4** Aug 2017 – Present

*Coursework*: RF Systems and Hardware EE567, Analog-Mixed Integrated Circuits I EE536A,

Analog-Mixed Integrated Circuits II EE536B, Communications Integrated Circuits EE632, VLSI System Design EE577A,

Quantum Mechanics EE539, Solid State Processing and Integrated Circuits Laboratory EE504

**Ain Shams University, Faculty of Engineering**, Cairo, Egypt

**M.Sc. with thesis**, Electrical Engineering, **GPA 3.54/4** Oct 2013 – May 2017  
 *Coursework:* Analog IC Design, Digital IC Design, RFIC Design, Power Management IC Design, and High-Speed Serial Links.

*M.Sc. thesis:* “A Low-power High-speed ADC-based Equalizer for Serial Links.”

**Alexandria University, Faculty of Engineering**, Alexandria, Egypt

**B.Sc.**, Electrical Engineering, Electronics Major, 93.44% equivalent to **GPA 3.96/4** Sept 2008 – July 2013  
 Distinction with degree of honor (5 years distinction), **Valedictorian** of a 335-student class.

**WORK EXPERIENCE**

**The University of Southern California, Viterbi School of Engineering,** Los Angeles, CA

*Graduate Research Assistant* Aug 2017 – Present

* Working on DARPA **WARP** program.
* Started working on DARPA **MIDAS** and **POSH** Projects. Jan 2019
* Served as a Teaching Assistant for EE 536A w/ prof. Hossein Hashemi Fall 2019

**Skyworks Inc.,** Newbury Park, CA

*Analog-Mixed IC Design Engineer Intern* June 2018 – Aug. 2018

* Worked in Advanced Mobile Solutions Division.
* Worked on PA Digital Controller and Bias Circuits.

**Silicon Vision (Si-Vi), Synopsys Inc.,** Cairo, Egypt

*Analog-Mixed IC Design Engineer* Dec. 2015 – July 2017

* Designed discrete-time and continuous-time comparators, and up-down counter.
* Worked on Analog verification of IO pads, loop-filter, VCO, feedback divider and calibration divider.

**Integrated Circuits Lab (ICL), Ain Shams University,** Cairo, Egypt

*Graduate Research Assistant* Sept. 2013 – Nov. 2015

* Worked on a low-power high-speed serial link ADC-based receiver.
* Responsible for the design of an ultra-low-power ADC and a front end CTLE equalizer.

**Alexandria University, Faculty of Engineering**, Alexandria, Egypt

*Assistant Lecturer/Teaching Assistant*  Sept. 2013 – July 2017

* Taught full lectures and labs in Circuits Analysis, Logic-Design, Electronics I and II,

Analog IC Design, Solid-State Physics, Solid-State Devices, 8086/8088 Microprocessor basics I and II.

**CONSULTIX Systems,** Cairo, Egypt

*RF Board Level Design Engineer Intern* Jan. 2014 – Feb. 2014

* Worked on Rectenna RF-DC Conversion and gained experience in ADS software.

**Si-Ware Systems (SWS),** Cairo, Egypt

*Application Engineer Intern*, ASIC solutions division Aug. 2012 – Sept. 2012

* Worked on testing SWS chips and gained experience in LabVIEW software.

**CURRICULUM PROJECTS**

***Major Design Projects:***

*“A 20-GHz Non-Uniform Sub-Sampling RX featuring Non-Uniform DT-FIR Filter” (****Individual****)* Present

* Doing system and architecture level design.
* Designed the signal-chain and the clocking system.

*“A 26-GHz SHS Digital PA” (****Team of 3****)*April. 2020 – June. 2020

* Verified AM and PM input buffers and helped in the chip layout.
* Designed and verified some digital control circuits.

*“A 6-GHz Sub-Harmonic-Switching (SHS) Digital Power-Amplifier (PA)” (****Team of 3****)* May. 2019 – Sept. 2019

* Verified AM and PM input buffers and helped in the chip layout.
* Designed and verified EM structures in Cadence Virtuoso and HFSS.

*“A 26.88-GHz Non-Uniform Sub-Sampling RX for mm-Wave Applications” (****Team of 2****)* Feb. 2019 – Nov. 2019

* **Taped-Out** in TSMC 28nm technology. May 2019
* Designed the signal-chain including mm-Wave input buffers, sub-sampling master-slave sampling network and output buffers.
* Helped in chip-measurements

*“An 8-bit Ultra-Low-Power SAR ADC for Bio-signals Applications” (****Individual****)*Oct. 2017 – Feb. 2019

* **Taped-Out** Ultra-Low-Power 100-nW 8-Bit SAR ADC using TSMC 65nm technology. Sept. 2018
* Built the ADC-PCB Test Board and carried out the measurements.

*“Designing a General-Purpose Microprocessor and Modeling an ASIC Accelerator for BNN” (****Team of 3****)*Oct. 2018 – Nov. 2018

* Built 4-Stage 16-bit Pipeline Microprocessor.
* Modeled the whole CPU in Python and tested Schematics and Layout for Functionality.
* Modeled BNN in Python and used the designed CPU with modifications for BNN Processing Acceleration.

*“A 75-dB 100-MHz Signal-Bandwidth Continuous Time Delta-Sigma ADC” (****Team of 2****)* March 2018 – April 2018

* Built system-level simulations using both Verilog-A and MATLAB for CIFF and CIFB architectures.
* Built 1.5bit Quantizer and 1.5bit Feedback DAC.

*“A Low-Power 12-Gbps Multi-Standard SERDES Transceiver” (Funded by ITIDA) (****Team of 3****)*Sept. 2013 – Nov. 2015

* Designed an ultra-low-power ADC and a Discrete-Time Linear Equalizer (DTLE).
* Modeled a Digital DFE and an adaptive CTLE
* **Finished post-layout** simulations for 20-Gbps 15.5-mW ADC in UMC65 and built the chip I/O Pad ring.

*“High-Speed Serial Link Transceiver for 10Gbase-KR Standard Using a 65-nm CMOS Process” (****Team of 8****)* Sept. 2012 – June 2013

* Modeled a time-interleaved Flash ADC using MATLAB Simulink
* Designed a 4-bit 10GS/s time-interleaved Flash ADC, Thermometer to binary digital encoder, and 1:16 Demultiplexer.
* Designed the digital RX system level.

***Mini Design Projects:***

*“512-Bit SRAM Architecture Design” (****Individual****)* Sept. 2018

* Build 4 banks of SRAM, Row Decoder, Column Decoder, Sense Amplifier
* All schematics to Layout, PEX and post-layout simulations

*“A Differential 3.5-GHz Voltage Controlled Oscillator” (****Individual****)*  April 2018

* Designed an LC-tank based Oscillator with 20% tuning range.
* Used digital bits and a varactor to tune the oscillation frequency.

*“A Differential Switched-Capacitor Residue Amplifier for 12-bit 100 MS/s ADC” (****Individual****)*  April 2018

* Analyze the different non-idealities in the SC amplifier and their effects.

*“Zero/Low IF Wireless Receiver Frontend: LNA + Harmonic-Reject Quadrature Mixer” (****Individual****)*  March 2018

* Designed an HRM using multi-phases clock.
* Achieved HR3 of 40.5dB, HR5 of 54.3dB and power of 9mA for the LNA and the Mixer.

*“12-bit 200-MS/s 5-GHz Bandwidth Track and Hold Circuit” (****Individual****)*  March 2018

* Built a driver for the sampling circuit
* Used a bootstrapped switch to get low distortion as possible
* Achieved input, SNDR of and SFDR of

*“An Inductor-less Wideband Low Noise Amplifier” (****Individual****)*  Feb. 2018

* Designed a Gm-boosted LNA using feedforward cancellation technique.
* Designed for low-gain and high-gain operation.

*“A Rail-to-Rail Input / Output Current-Recycling Folded Cascode OTA in 45nm Process” (****Individual****)*  Nov. 2017

* Designed a two-stage OTA with a rail-to-rail input and output.
* Used miller and feedforward compensation.
* Achieved gain of GBW of , while consuming

*“A Design of eDRAM System Architecture” (****Team of 3****)* April 2015 – June 2015

* Designed 4T and 3T1D eDRAM cells, Sense Amplifier, Column Tree Decoder, and NOR Row Decoder.
* Used Fin-FET Verilog-A model from EECS Berkeley open library.

*“A Design of Full 6-Gbps SERDES Link: Channel-Characterization, TX and RX” (****Team of 3****)* Dec. 2014 – Jan. 2015

* Designed CTLE, VGA, Sampler and SR Latch.

*“A Design of SC Buck DC-DC Step-Down Converter” (****Team of 3****)*  July 2014 – Aug. 2014

* Designed Multi-ratio (1, , , ) adaptive SC DC-DC converter to down convert 2.5V nominal line to 1.8V
* 38mV output ripples for 200mV input ripples, 30mΩ ESR and accuracy of 20mV

*“A Design of Wideband Low-Noise Amplifier (LNA)” (****Individual****)* April 2014 – May 2014

* Designed a highly linear LNA with 18.25dB gain, 1dB NF, 2.2dBm IIP3.
* The total power consumption is 4.3mA. The LNA is operating from 200MHz to 2.45GHz

*“Designing a Spiral, Coplanar and Microstrip Inductors Using Sonnet” (****Individual****)* April 2014 – May 2014

* Designed different types of integrated inductors with different quality factors.
* Gained experience in Sonnet software.

*“A Model of a Simple System Level for Bluetooth System Using Simulink” (****Individual****)* Feb. 2014 – March 2014

* Modeled a simple and abstractive Bluetooth system using ADC and Phase domain ADC in MATLAB.

*“Design and Characterization of a CMOS 8‐bit Microprocessor Data Path” (****Team of 5****)* March 2013 – June 2013

* Designed the behavioral model of an 8-bit microprocessor using Verilog.
* Designed the barrel shifter, latches and flip-flops & their layout using L-Edit.

*“System Level Design of a Pipeline ADC” (****Individual****)* Sept. 2012

* Modeled a 1.5bit M-DAC based Pipeline ADC using MATLAB Simulink.
* Investigated building open-loop and closed-loop amplifier in each pipeline sub-stage.

*“Behavioral Modeling for Serial Data Receiver Using VHDL” (****Individual****)* April 2011 – May 2011

* Designed a behavioral serial data RX that receives data chunks of 10 bits from a serial data bus.

RX was modeled Using Xilinix, Modelsim and written in VHDL.

**TECHNICAL SKILLS**

* **Simulation Tools:** Cadence Virtuoso, MATLAB and Simulink, ADS, Synopsys analog flow, Sonnet, LabVIEW,

Xilinx ISE, Quartus, Modelsim, PCB skills, Multisim, and Mentor Graphics (ELDO), HSPICE,

* **Layout:** Calibre (DRC, LVS, PEX), and L-Edit
* **Programming:** Verilog-AMS, VHDL, Shell Scripting, Python, SKILL, C, and Assembly (for x86 series and MCS-51 family)
* **Lab instruments**: LPFKS62, Network Analyzer, NI-DAQ, Temperature Chamber, Oscilloscope,

Multimeter, logic analyzer, and Function generator

* **Editing:** LATEX, Inkscape, and MS-Visio
* Underlined terms refer to a beginner-level experience

**PUBLICATIONS & PREPRINTS**

1. Aoyang Zhang, **Mostafa Ayesh**, Soumya Mahapatra and Mike S. W. Chen, “A 24-28 GHz Concurrent Harmonic and Subharmonic Tuning Class E/F2,2/3 Subharmonic Switching Power Amplifier Achieving Peak/PBO Efficiency Enhancement” CICC 2021.
2. Aoyang Zhang, Ce Yang, **Mostafa Ayesh** and Mike S. W. Chen, “*Current-Mode SHS sub 6-GHz PA,”* ISSCC 2021.
3. Ce Yang, **Mostafa Ayesh**, Aoyang Zhang and Mike S. W. Chen, “*A 29-mW 26.88-GHz Non-Uniform Sub-Sampling Receiver Front-End Enabling Spectral Alias Spreading,”* RFIC 2020.
4. **M. M. Ayesh**, S. Ibrahim and M. M. Aboudina, “*Design and Analysis of an Ultra-Low-Power Charge-Steering Based StrongARM Comparator*,” ICM, December 2016.
5. **M. M. Ayesh**, “*A Low-power High-speed Charge-steering ADC-based Equalizer for Serial Links*,” ICECS, M.Sc/Ph.D. Forum, December 2015.
6. **M. M. Ayesh**, S. Ibrahim and M. M. Aboudina, “*15.5-mW 20-GSps 4-Bit Charge-Steering Flash ADC*,” MWSCAS, pp.33-36, August 2015.

**Preprints:**

* + **Mostafa M. Ayesh**, Sameh Ibrahim and Mohamed M. Aboudina, “A Low-Power 20-Gb/s Discrete-Time Analog Front-End for ADC-Based Serial Link Equalizers,” preprint arXiv:1902.00233, Jan 2019.

**AWARDS**

* Recipient of **CICC 2019 Student Travel Grant Award** (2019)
* Recipient of **Annenberg Fellowship**, USC Viterbi School of Engineering (2017-2021)
* Recipient of a full scholarship throughout M.Sc. studies. (2013-2016)
* Third place in M.Sc. Forum of the 2015 IEEE International Conference on Electronics, Circuits, and Systems for: “A Low-Power High-Speed Charge-Steering ADC-Based Equalizer for Serial Links”.
* Recipient of Alexandria University annual academic **distinction award**. (2009-2013)

**Extra Academics**

* ***First in Class*** in RF Systems and Hardware **EE567**, Analog-Mixed Integrated Circuits I **EE536A**, Analog-Mixed Integrated Circuits II **EE536B**, Communications Integrated Circuits **EE632**, VLSI System Design **EE577A** and Solid-State Processing and Integrated Circuits Laboratory **EE504**
* Audit: **USC CS570**: Algorithm Design in Summer 2019
* Audit: **USC** **EE483**: Introduction to Digital Signal Processing in Fall 2019
* Audit: **USC** **EE552**: Asynchronous VLSI Design in Spring 2020
* Audit: **USC** **EE505**: Analog, Mixe, RF IC Tape-out in Summer 2020

**TECHNICAL SERVICES**

* Reviewed papers for CICC-2019, ISSCC-2019, VLSI-2019, CICC-2020, ISSCC-2020, the IEEE International Symposium on Circuits and Systems (ISCAS) 2017, MWSCAS-2017, and Springer-Ain Shams Journal.
* Reviewed projects for IEEE Egypt section in 2015 EED (Egyptian Engineering Day).

**EXTRACURRICULAR ACTIVITIES**

**IEEE CICC 2019 Volunteer** April 2019

**VLSI-Egypt – Alexandria Section NGO**, Alexandria, Egypt. Nov 2013 – Dec 2016

*Founder and Chairman*

**EgyptScholars – Alexandria Student Branch NGO**, Alexandria, Egypt Sept 2013 – Mar 2015

*Founder and Chairman*

**IEEE – Alexandria Student Branch – SSCS**, Alexandria, Egypt Sept 2013 – Mar 2015

*Instructor for Basic Electronics & Analog Design courses*

**EWEB NGO**, Alexandria, Egypt Sept 2013 – Dec 2014

*Instructor for Basic Electronics & Analog Design courses*