Ravi teja Lakkireddy

Masters student (EE) at USC

1 June 1997

lakkired@usc.edu

+1 2133488745

www.linkedin.com/in/ravi1997

Education

M.S. in Electrical Engineering - VLSI | Jan 2021 - Cont. | GPA - 4.0 | University of Southern California

Bachelor of Technology: Electronics and Communication Engineering | 2014-18 | 88% GITAM University, Andhra Pradesh, India.

Skills

EDA tools :
- Cadence Virtuoso
- Synopsys HSPICE
- CustomSim
- RedHawk

Simulation Tools :
- Arduino
- LabVIEW
- Ansys-HFSS

Protocols :

Worked on:
- eDP
- DDI
- MIPI

Good knowledge on:
- I2C
- SPI
- UART
- USB

Languages:
- C, C++
- Matlab
- VHDL
- Verilog
- Basics of Java and SQL
- Python
- Perl

Work Experience and Internships

Since Aug'21 Analog Design Engineer Intern — Information Sciences Institute
- Working on Designing of DARPA's Artificial Intelligence based Low power In-Pixel computing Camera for object detection
- Designing Optical sense amplifier for Boolean optical in-memory computing

Since Aug'18 Analog Design Engineer — Eximius Design India Pvt Lmt, India
Designed and developed High speed SERDES IPs and IO Circuit (DDR7) Designs and was exposed to every stage of the project from Porting of design to Power Delivery Validation.Gained experience in the Design and verification of TX, RX, and Clock distribution blocks in high-speed SERDES and acquired extensive knowledge on architectures of PLL, DLL, Ring Oscillator, ADC, DAC circuits.Well versed with Cadence and designing in TSMC- 5nm technology.

Jan-July'18 Apprentice Trainee — Eximius Design India Pvt Lmt, India
Training Project : Designed and implemented various Architectures of critical blocks - Ring Oscillator, Delay locked loop(DLL), Phase Frequency Detector(PFD), Low Drop out(LDO) - budgeting parameters like Power and Performance. And present the merits and demerits of each Architectural Design

Summer'17 Research Intern — Defence Research and Development Organization, India
Designed "Microcontroller Based Antenna Positioning System" Hardware and software has been integrated as a single unit tailored for missile tracking and the system is tested through simulation

Coursework Taken and Project - Masters

EE536A Analog Integrated Circuits — On going
Designing and analyzing analog integrated circuits for wide range of applications such as wireless and wired communications, biomedical implants, controls, computation, sensing, imaging, etc

EE560 Digital System Design — GPA - 4.0
Projects: Out-Of-Order instruction-executing CPU, Multi-threaded Multi-core CPU, PCIe (PCI express) Datalink layer and Physical layer

EE577 VLSI System Design — GPA - 4.0
Project: Flash SRAM: Designed a dual Port SRAM with hybrid operating mode including memory access and In-memory computation with an effective data rate of 4.8 GHz and leakage power of pico order

EE457 Computer Systems Organization — GPA - 4.0
Gained knowledge about logical design of CPU (CU and DPU)

EE590 Directed Research | Advised by Dr. Alice Parker — CR
Designed and Analyzed Farquhar's spiking circuit that generates action potential by modeling ion channels on Cadence Virtuoso

Achievements

May'21 USC Viterbi MS Honors Fellowship — USC Viterbi School of Engineering
Admitted into USC Viterbi MS Honors Fellowship program (<%5 admitted)

Jan'19 THE BEST TEAM AWARD — Eximius Design India Private Limited
Awarded 'THE BEST TEAM' award for designing combo display port for Intel

Feb'17 Winner in Electronics Premier League|EPL'17 — IETE Student Chaptper
Awarded first position for championing in Electronics Circuit Design quiz computation

Feb'17 First - Maze solver Event — IETE, Student chapter
Awarded with first position for building Smart Robot, SPACE-BOT, detecting the shortest path, avoiding obstacles, and reaching the target in lesser time

Ravi teja Lakkireddy

Masters student (EE) at USC

1 June 1997

lakkired@usc.edu

+1 2133488745

www.linkedin.com/in/ravi1997

Education

M.S. in Electrical Engineering - VLSI | Jan 2021 - Cont. | GPA - 4.0 | University of Southern California

Bachelor of Technology: Electronics and Communication Engineering | 2014-18 | 88% GITAM University, Andhra Pradesh, India.

Skills

EDA tools :
- Cadence Virtuoso
- Synopsys HSPICE
- CustomSim
- RedHawk

Simulation Tools :
- Arduino
- LabVIEW
- Ansys-HFSS

Protocols :

Worked on:
- eDP
- DDI
- MIPI

Good knowledge on:
- I2C
- SPI
- UART
- USB

Languages:
- C, C++
- Matlab
- VHDL
- Verilog
- Basics of Java and SQL
- Python
- Perl

Projects

Jan'18 — Training Project — Internship Project - EXIMIUS

Designed and implemented various Architectures of critical blocks - Ring Oscillator, Sense Amplifier, Delay locked loop(DLL), Phase frequency Detector(PFD), Low Drop out(LDO)
- Performed statistical, qualitative and quantitative analysis and budgeting parameters like Power and Performance. And present the merits and demerits of each Architectural Design
- Summarized search results by preparing written reports, graphs, fact sheets and tables.
- Developed macros, special formulas and other actions to produce reliable and consistent statistical reviews.
- Planned, modified, and executed research techniques, procedures and tests.
- Conducted meticulous research to identify information and answer multifaceted questions.
- Validated incoming data to check information accuracy and integrity while independently locating and correcting concerns.

Jun'18 — Design and Development of Combo Display port - 10nm — INTEL

SERDES IP which supports eDP, MDFI, HDMI and DP protocols
- Responsible for the ICOMP calibration and RCOMP calibration for impedance matching by generating respective codes using COMP CBB calibration.
- Worked on Macros to formulate the thermcodes accordingly and ease the verification across PVT corners (semi-automated approach to reduce round about time).
- Developed, tested and assessed alternative design models and processing methods.
- Worked on MIPI LPTX to check functionality and spec validation for different parameters like Impedances, Linearity, VOH, VOL, Slopes, Slew rate & Pulse width.
- Worst case identification, top level simulation, Monte Carlo analysis, and simulation data analysis.
- Strong understanding of circuit fundamentals and impact of PVT variation on design performance.

Nov'19 — Design and Development of 3.2GBps SERDES IP - 10nm — INTEL

Working on Design and development of 3.2GBps SERDES IP - 10nm
- Owned and executed verification of critical blocks like Sense Amplifier (SAL) , Vref Ladder in RXCBB and worked with layout designers and other cross-functional teams like RTL and PD for sign-off.
- Supported the fixture of Sync, Slice CBB.
- Worked on Macros to formulate and find setup and hold timing window of Sense Amplifier.
- Worked on all phases of design analysis including functional, static timing and electrical sign-off.
- Demonstrated capabilities in using top level to block and bottoms up block to top level methodology to define interdependency between blocks and achieve convergence for top level specs
- Worked closely with Layout team for Physical layout management, signal grounding and routing trade-offs and die area optimization.

Extra Curricular

Core-Member at IETE:- Organized various technical competitions, events & workshops | Member of 'Tech-Hub' which concentrates on doing innovative projects.

Active Member at IEEE:- Has participated in various Presentations, Project Expos, Technical Events and Competitions in the fests organized by IEEE.

Volunteer at NSS & KEN NGO:- Co-organized and participated in various events like Toofan Fund-raising, Blood Donation, Pulse Polio, Supporting Orphan children