Arash Fayyazi

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EDUCATION

Ph.D. in Electrical Engineering, University of Southern California (USC)	GPA: 3.9/4 Aug 2017 – August 2022(EGD)
M.Sc. in Computer Science University of Southern California (USC) *Coursework*: Database Systems (CSCI585), Analysis of Algorithms (CSCI570), Deep Learning and its Applications (CSCI 566), Foundations of Artificial Intelligence (CSCI 561), CSCI Special Topics: Computer-Aided Verification (CSCI 699), Scientific Computing and Visualization (CSCI 596), Information Retrieval and Web Search Engines (CSCI 572)	GPA: 3.8/4 Aug 2017 – May 2021
M.Sc. in Electrical Engineering University of Southern California (USC) *Coursework*: VLSI System Design (EE577A), Computer-Aided Design of Digital Systems (EE681), Mathematical Foundations for System Design (EE599), Introduction to Programming Systems Design (CSCI 455), Probability for Electrical and Computer Engineering (EE503)	GPA: 4/4 Aug 2017 – May 2020
M.Sc. in Electrical Engineering – Electronics, Minor in Circuits and Systems University of Tehran (UT) *Coursework:* Custom implementation of DSP systems, Advanced Topics in Computer Architecture – Chip Multiprocessors, pre- and post-silicon debugging of digital systems, VLSI System Design	GPA: 4/4 August 2014 – January 2017

SKILLS

- **Programming languages:** C/C++/C#, Python, and JAVA.
- **Version Control:** Git.
- **Hardware Languages:** Verilog, VHDL, SystemVerilog, SystemC.
- **Databases:** SQL, MySQL, Postgres, PostGIS.
- **Tools:** Xilinx Vivado (HLS), Xilinx SDAccel, MATLAB, Cadence and Synopsys tools, Quartus, Keras, TensorFlow, Pytorch, TinkerPop.
- Worked on online cloud platform, viz AWS and GCP**.**

HONORS AND AWARDS

Selected as a recipient of the DAC young fellows poster presentation awards.	July 2020
Awarded DAC Young Fellowship for attending 57th ACM/IEEE Design Automation Conference	July 2020
Awarded Student Travel Support for attending International Superconductive Electronics Conference	July 2019
Ranked the third student among 28 students of Electronics Engineering - Major – Circuits and Systems	2014 – 2017
Ranked the first student among 40 students of Electronics Engineering	2010 – 2014
Ranked the first student among 120 students of Electrical Engineering	2010 - 2014
Ranked the 7th in Robocup IranOpen 2008 International Competition in Qazvin, Iran (League: Soccer 2D simulation)	April 2008
Ranked the second team in the Second National Robocup (Soccer 2D Simulation) Competition for Students	March 2008
Member of **Exceptional Talents** in Ferdowsi University of Mashhad	2010 – 2014
Honorary Admission to University of Tehran Master program as Exceptional Talent, without national entrance exam	2014
Awarded Ferdowsi University of Mashhad scholar as the **distinguished B.Sc. graduate** of the year	2014

PROJECTS

- **Low-cost FPGA-based CNN Acceleration [Pytorch, Python, Verilog, C/C++, OpenCL]:** May 2019-Current
  - Developed a Compiler for scheduling and mapping the high-level modeling of CNNs on FPGA.
  - Designed a memory-efficient hybrid accelerator architecture to support various precision, including 16-bit fixed point and binary precision.
  - Optimized a target DNN for a given dataset and maps major parts of computations in the DNN to ultra-low-latency, low-cost, fixed-function, combinational logic blocks.

- Introduced and implemented a parallel version of logic minimization algorithm by taking advantage of the computing capabilities of GPUs to achieve a considerable speedup compared to existing serial implementations.

❖ **Tool Flow for enabling Processing-In-Memory for Memristive Crossbars [Python, SPICE]:** May 2019-Current
- Implemented a novel logic synthesis approach with a dedicated mapping strategy tailored on MAGIC crossbars.
- Significantly improved both the average computational latency (2.12x) and area (1.38x).

❖ **Deep-learning-based CAD tools [C++, Python, Tensorflow, Verilog]:** Mar 2018-Current
- Created a tool for efficiently recognizing the functionality of a circuit leveraging deep learning.
- Proposed a convolutional neural network (CNN)-based circuit representation.

❖ **Post-synthesis verification of superconductive electronic circuits [C++, Python, SystemVerilog]:** Jan 2018-Current
- Presented a novel graph representation of the beyond-CMOS circuit to be utilized in formal methods.
- Successfully implemented a novel learning-based UVM-compliant verification framework.
- Developed a model checker for SFQ circuits using formal techniques which offers an automated process that constructs a SystemVerilog testbench consisting of formal assertions to verify the SFQ specific properties of the circuits and produce system correctness results and counterexamples using model checking.
- Presented elegant and conceptual SystemVerilog models for SFQ and AQFP gates and the circuits that interface between them, compatible with standard delay format and commercial simulators.

❖ **Design and implementation of neuromorphic circuits [MATLAB, SPICE, Python]:** Aug 2015-Current
- developed ultra-low-power smart sensor using high-speed NN-based ADC/DAC.
- Actively working on developing efficient training algorithms and CAD tools to facilitate memristive-based circuit implementation.
- **M.Sc project:** Designed and implemented neuromorphic circuits as an analog coprocessor for a digital processing system, developed ultra-low power smart sensor using high-speed ADC/DAC, developed efficient training algorithms and CAD tool to facilitate memristive-based circuit implementation.

❖ **Approximate Computing [MATLAB, Verilog]:** August 2014-August 2015
- Developed a high-speed yet energy-efficient approximate divider; Successfully implemented in hardware.
- 14x and 300x smaller delay and energy consumption compared to the Radix-2 SRT

ACADEMIC EXPERIENCE & PROFESSINAL SERVICES

❖ Closely mentoring ten graduate students and involved them with the research, including functional verification of superconductive electronic circuits, improving the functional coverage utilizing machine learning algorithm, publish results in ISQED'19 and GLSVLSI'19. Jan 2018- Current

❖ Teaching Assistant (Electronic II, Computer Architecture) & Verilog Instructor (Computer Architecture laboratory). Aug 2013- May 2016

❖ Reviewer of IEEE transactions on neural networks and learning systems journal, IEEE Access journal, IEEE Transactions on Applied Superconductivity, Springer CCF Transactions on High Performance Computing, IEEE Transactions on Electron Devices, IEEE Transactions on Circuits and Systems II: Express Briefs, and IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Jan 2019- Current

SELECETED PUBLICATIONS

❖ qEC: A Logical Equivalence Checking Framework Targeting SFQ Superconducting Circuits, *ISEC 2019.*

❖ Deep Learning-Based Circuit Recognition Using Sparse Mapping and Level-Dependent Decaying Sum Circuit Representations, *DATE 2019*.

❖ CSrram: Area-Efficient Low-Power Ex-Situ Training Framework for Memristive Neuromorphic Circuits Based on Clustered Sparsity, *ISVLSI 2019.*

❖ A Hybrid Framework for Functional Verification using Reinforcement Learning and Deep Learning, *GLSVLSI 2019.*

❖ OCTAN: An On-Chip Training Algorithm for Memristive Neuromorphic Circuits, *IEEE TCAS-I 2019*.

❖ SynergicLearning: Neural Network-Based Feature Extraction for Highly-Accurate Hyperdimensional Learning, *ICCAD 2020*.

❖ Inverter-based Memristive Neuromorphic Circuit for Ultra-low-power IoT Smart Applications, *A book chapter published in IET Book on Hardware Architectures for Deep Learning, 2020*.

❖ NullaNet Tiny: Ultra-low-latency DNN Inference Through Fixed-function Combinational Logic, *FCCM 2021.*