REZWAN A RASUL

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RESEARCH TOPIC

Energy-efficient implementation of machine-learning algorithm using application specific IC

EDUCATION

PhD in Electrical Engineering — August 2016 - Now
CGPA: 3.76/4.00
University of Southern California, CA, USA

ME in Physical Electronics — April 2014 – March 2016
CGPA: 2.87/3.00
Tokyo Institute of Technology, Tokyo, Japan

BE in Electrical and Electronics Engineering — April 2010 – March 2014
CGPA: 2.91/3.00 (ranked 2nd in a class of 100)
Tokyo Institute of Technology, Tokyo, Japan

RESEARCH EXPERIENCE

1. **Article:**
   i. M Hassanpourghadi, R. A. Rasul, MSW Chen, "A Module-Linking Graph Assisted Hybrid Optimization Framework for Custom Analog and Mixed-Signal Circuit Parameter Synthesis," ACM Trans. Des. Autom. Electron. Syst. 26, 5, Article 38 (June 2021), 22 pages.
2. **Conference paper:**
   i. R. A. Rasul, MSW Chen, "A 128×128 SRAM Macro with Embedded Matrix-Vector Multiplication Exploiting Passive Gain via MOS Capacitor for Machine Learning Application," IEEE Custom Integrated Circuits Conference (CICC), Apr. 2021.
   ii. R. A. Rasul, P. Teimouri and M. S.-W. Chen, "A time multiplexed network architecture for large-scale neuromorphic computing," 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), Boston, MA, 2017, pp. 1216-1219.
   iii. M. Hassanpourghadi, S. Su, R. A. Rasul, J. Liu, Q. Zhang, and M. S.-W. Chen, "Circuit Connectivity Inspired Neural Network for Analog Mixed-Signal Functional Modeling," 2021 58th ACM/EDAC/IEEE Design Automation Conference (DAC), Dec. 2021 (to appear)
   iv. J. Liu et. al. ""From Specification to Silicon: Towards Analog/Mixed-Signal Design Automation using Surrogate NN Models with Transfer Learning" ICCAD 2021 (to appear).
3. **Poster:**
   i. R. A. Rasul, M. S.-W. Chen, " A low power in-memory matrix-vector multiplier for machine learning classifier," 10th Annual EE Research Festival, Nov. 2019
   ii. R. A. Rasul, P. Teimouri and M. S.-W. Chen, "A time multiplexed network architecture for large-scale neuromorphic computing," 9th Annual EE Research Festival, Nov. 2018

4. **Master's thesis:** A Study of SAR ADC with wide input voltage range Jan 2015 – March 2016
   Supervisor: Prof. Akira Matsuzawa and Prof. Kenichi Okada
   Designed and laid out two 12-bit, 10MSps, 0-5V differential input synchronous SAR ADCs for automotive sensor application.
5. **Undergraduate thesis:** Investigation of low drop-out (LDO) regulator as a power control circuit in SAR ADC September 2013 – March 2014
   Supervisor: Prof. Akira Matsuzawa and Prof. Kenichi Okada
6. **Research Assistant:**
   a. Dr. Mike Chen research group, University of Southern California
   Design of mixed-signal, energy-efficient accelerator for Deep Neural Network (DNN)
   Aug 2016 – Present
   b. Matsuzawa and Okada Lab, Tokyo Institute of Technology
   Design of amplifier for interpolated pipeline ADC April 2013 – September 2013

MAJOR ACADEMIC PROJECTS:

- Design of a fully differential amplifier for switched capacitor multiplying digital to analog (MDAC) stage Fall 2016
- Design of a general-purpose microprocessor using software and hardware components Fall 2016
- Design of a wideband low-noise amplifier, harmonic reject quadrature mixer and differential voltage-controlled oscillator Spring 2018

HONORS AND AWARDS

- Monbukagakusho Fellowship for Master's granted by Ministry of Education, Culture, Science, Sports and Technology (MEXT), Japan April 2014 – March 2016
- Electrical Engineering Academic Award for undergraduate merit position by IEEE, Japan March 2014
- Monbukagakusho Fellowship for Undergraduate by MEXT, Japan April 2009 – March 2014
- Merit Scholarship awarded by Secondary and Higher Secondary Education Board, Bangladesh for outstanding performance in public exams of 8^{th}, 10^{th} and 12^{th} grade 2004 2006 and 2008

WORK EXPERIENCE

- **Internship:**
  1) NEC Corporation Summer 2012
     Inspected security of a drive encryption system
  2) Sony Corporation Summer 2012
     Measured and compared performance of camera antennas in various frequency regions
- **Teaching and Mentoring:**
  1) Mentor of the SHINE program at University of Southern California Summer 2018
     Guided a high school senior to train and test quantized neural network.
  2) TA of EE 348L at University of Southern California Fall 2018
     Graded homework and instructed PCB design labs
  3) TA of SAR ADC training session, organized by Matsuzawa and Okada Lab March 2015
     Assisted participants to setup testbench and perform ADC simulation using LTSpice

4) TA of EEE laboratory 3 (junior years undergraduate course) Autumn 2014
   Explained theory, assisted in VHDL coding, set up FPGA for distance measurement
5) TA of Global Scientists and Engineering Course Autumn 2014
6) Tutor of YSEP exchange student at Matsuzawa and Okada Lab Autumn 2014
   Assisted in MATLAB simulation of PLL

TECHNICAL SKILLS

- Simulations Tools: Cadence (Virtuoso Schematic Editor, Layout Editor, Analog Design Environment, Spectre Circuit Simulator), MATLAB, LTspice, PSpice, Verilog-A
- Programming: Python, C/C++, Java, Unix

CERTIFICATION

- JLPT (Japanese Language Proficiency Test): Level N1