HSIANG-CHUN CHENG

Curriculum Vitae/Resume

+1 (213) 705-6775 hcheng15@usc.edu Personal Web. rmp850902 Hsiang-Chun Cheng

RESEARCH INTERESTS

- **Analog/RF Integrated Circuit Design**
- **Mixed-Signal Circuit Design**

EDUCATION

B.S. in Electrical Engineering — Sept. 2015 - June 2019

Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan

– Relevant Coursework: Analog Integrated Circuits Design, RF Microwave Wireless Systems, Principle of Communications, *Advanced Digital Signal Processing, *Theory and Application of Phase-Locked Loop (*: Graduate-level courses)

Ph.D. in Electrical Engineering — Jan. 2021 - present

Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, CA

RESEARCH EXPERIENCE

High-Speed Circuits Lab, National Taiwan University — Sept. 2017 - Oct. 2019

Advisor: Tai-Cheng Lee, *Professor*

Topic: Low-Power 32.768-kHz Crystal Oscillator

- Designed a self-charged crystal oscillator with pulse regulating feedback loop under a single 1-V power supply
- Proposed a pulse regulator that adaptively adjusts the energy injection time
- Analyzed the behavior of pulse injection and verified the analytical expression of locked amplitude
- Achieved 65.6% power reduction with process variations in a standard 40-nm CMOS process

PUBLICATIONS

[1] **H. -C. Cheng**, Y. -H. Yang and T. -C. Lee, "Analysis and Design of a Self-Charged Crystal Oscillator with Pulse Regulating Feedback Loop," *2020 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, Hsinchu, Taiwan, 2020, pp. 1-4 [link]

TRAINING

CMOS RFIC Design and Implementation — Feb. 2019

5-GHz Low Noise Amplifier Design in 0.18-μm CMOS, Taiwan Semiconductor Research Institute (Hsinchu), Taiwan

- Completed tape-out and on-wafer measurement [PDF]

Cell-Based Digital IC Design and Implementation — Aug. 2019

Gravity Center Calculator Design in 0.18-μm CMOS, Taiwan Semiconductor Research Institute (Hsinchu), Taiwan

- Completed tape-out and measurement [PDF]

SELECTED PROJECTS

Theory and Application of Phase-Locked Loop

A Simulation of Sub-Sampling Phase-Locked Loop [PDF]

- Studied and designed a 2.21-GHz sub-sampling phase-locked loop (SSPLL) in 0.18-μm CMOS
- Compared the output phase noise between the SSPLL and classical PLL
- Improved overall power consumption through an architectural change in the first-stage reference buffer

Analog Integrated Circuits Design

Design of a Two-Stage Differential Operational Amplifier [PDF]

- Demonstrated a detailed design of fully-differential telescopic op-amp in 0.18-μm CMOS

TECHNICAL SKILLS

Programming Languages: Matlab, Verilog, Python, Verilog-A, HSPICE

Design Tools: Virtuoso, Spectre, Design Compiler, Calibre, ADS

OTHER EXPERIENCE

Community Service at Gang Xi Elementary School, Keelung, Taiwan — Sept. 2016 - July 2017

American Language & Culture Program in Silicon Valley, Stanford University, CA — Aug. 2017