Shiyu Su

Ming Hsieh Institute (MHI) Scholar, University of Southern California (USC)

Address: 3737-Watt Way, PHE404, Los Angeles, California 90089, United States

Cell: (213) 359-1863   Website: https://sites.google.com/view/shiyusu   Email: shiyusu@usc.edu

RESEARCH INTEREST

High-speed and high-resolution data converters, all-digital phase-locked loop, RF/mm-Wave transceivers, AI-assisted analog/mixed-signal design automation, analog/mixed-signal/bio-inspired computing, micro-unmanned vehicles.

EDUCATION

University of Southern California, Los Angeles, CA **2011-2013, 2013-2019**

University of London, London, UK **2010-2011**

Beijing University of Posts and Telecommunications (BUPT), Beijing, China **2007-2010**

TEACHING EXPERIENCE

USC, EE505: Analog, Mixed Signal, and Radio-Frequency Integrated Circuit Tape-out – **Instructor** **2021**

USC, EE479: Analog Integrated Circuit Design – **Teaching Assistant** **2015**

RESEARCH EXPERIENCE

IARPA, Microelectronics in Support of Artificial Intelligence (MicroE4AI) Program – Designer **2021-present**

DARPA, Millimeter Wave Digital Arrays (MIDAS) Program – Designer **2018-present**

DARPA, Posh Open Source Hardware (POSH) Program – Designer **2018-present**

NSF, Spectrum Efficiency, Energy Efficiency, and Security (SpecEES) Program – Designer **2017-2018**

Google, Advanced Technology and Project (ATAP), Radio Revolution (R2) Project – Designer **2016**

DARPA, Computational Leverage Against Surveillance Systems (CLASS) Program – Designer **2015**

ONR, Silicon-Based Monolithic Digital RF Memory Program – Designer **2013-2014**

HONORS

IEEE RFIC Best Student Paper Award (First Place) **2022-2023**

- Awarded annually by the Radio Frequency Integrated Circuits Symposium (RFIC) to three student papers.

Ming Hsieh Institute (MHI) Scholar **2019-2020**

- Awarded annually by the ECE department of USC based on research accomplishments and finalist talks.

IEEE Solid-State Circuits Society (SSCS) Student Travel Grant Award **2019-2020**

- Awarded annually by the SSCS to supporting student travel to SSCS-sponsored conferences

IEEE Solid-State Circuits Society (SSCS) Predoctoral Achievement Award **2017-2018**

- Awarded annually by the SSCS to a small number of promising graduate students around the world.

SELECTED TALKS & POSTERS

"Time-Approximation Filter for Direct RF Transmitter" for **RFIC workshop** in Denver, Colorado	**2022**
"Breaking the IC Design Boundaries" for the **University of Waterloo (interview talk)**, Canada	**2022**
"Breaking the IC and System Design Boundaries" for the **UC Davis (interview talk)**, CA	**2022**
"New Opportunities in Mixed-Signal Circuits" for the **University of Texas at Austin (interview talk)**, Texas	**2021**
"Software Defined Electronic Systems" for **Columbia University (interview talk)**, NYC	**2020**
"A Tri-level Time-Approximation Filter for direct RF Transmitter" for Qualcomm Atheros, San Jose	**2020**
"A SAW-Less Direct-Digital Radio Frequency Modulator" for ninth Research Festival, USC	**2019**
"Digital-to-RF Conversion Techniques for All-Digital Communication" MHI Scholar Presentation, USC	**2019**
"All-Digital Transmitters for 5G" for Newradio Technology Co., Ltd. (NRT), Shenzhen, China	**2019**
"A Direct-Digital RF Modulator with Time-Approximation Filter" for ninth Research Festival, USC	**2018**
"A 16-bit 12GS/s Multi-Mode Hybrid DAC" for Wireless SOC Team Apple, Cupertino, CA	**2018**
"High-Linearity Wideband DAC for All-Digital Transmitters" for Class EE 505, USC	**2016**

PUBLICATIONS

Postdoc (2019-2021):

[1] **Shiyu Su** and Mike Chen, "High-Speed Digital-to-Analog Converter Design Towards High Dynamic Range," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2022. **(Best Invited Paper Candidate)**

[2] Qiaochu Zhang*, **Shiyu Su*** and Mike Chen, "A Cost-Efficient Fully Synthesizable Stochastic Time-to-Digital Converter Design Based on Integral Nonlinearity Scrambling," in *2022 59th ACM/EDAC/IEEE Design Automation Conference (DAC)*, July 2022. (Accepted; *Qiaochu and Shiyu contributed equally to this work)

[3] Ce Yang, **Shiyu Su** and Mike Chen, "A Millimeter-Wave Mixer-First Receiver with Non-Uniform Time-Approximation Filter Achieving >45-dB Blocker Rejection," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2022. **(Best Student Paper Award – First Place)**

[4] **Shiyu Su** and Mike Chen, "SAW-Less Direct RF Transmitter with Multi-Mode Noise Shaping and Tri-Level Time-Approximation Filter," *IEEE J. Solid-State Circuits (JSSC)*, 2022.

[5] **Shiyu Su**, Q. Zhang, M. Hassanpourghadi, J. Liu, R.A. Rasul, and Mike Chen, "AMS Circuit Synthesis Enabled by the Advancements of Circuit Architectures and ML Algorithms," in *2022 27th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2022. **(Invited)**

[6] **Shiyu Su**, Q. Zhang, J. Liu, M. Hassanpourghadi, R.A. Rasul, and Mike Chen, "TAFA: Design Automation of Analog Mixed-Signal FIR Filters Using Time Approximation Architecture," in *2022 27th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2022.

[7] J. Liu, **Shiyu Su**, M. Madhusudan, M. Hassanpourghadi, S. Saunders, Q. Zhang, R. Rasul, Y. Li, J. Hu, A. K. Sharma, S. S. Sapatnekar, R. Harjani, A. Levi, S. Gupta and Mike Chen "From Specification to Silicon: Towards Analog/Mixed-Signal Design Automation using Surrogate NN Models with Transfer Learning," in *2021 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2021.

[8] Q. Zhang, **Shiyu Su**, C.-R. Ho, and Mike Chen, "A Fractional-N Digital MDLL with Background Two-Point DTC Calibration," *IEEE J. Solid-State Circuits (JSSC)*, 2021. **(Invited)**

[9] M. Hassanpourghadi, **Shiyu Su**, R.A. Rasul, J. Liu, Q. Zhang, and Mike Chen, "Circuit Connectivity Inspired Neural Network for Analog Mixed-Signal Functional Modeling," in *2021 58th ACM/EDAC/IEEE Design Automation Conference (DAC)*, Dec. 2021.

[10] **Shiyu Su** and Mike Chen, "A Time-approximation Filter for Direct RF Transmitter," *IEEE J. Solid-State Circuits (JSSC)*, 2021.

[11] Q. Zhang, **Shiyu Su**, C.-R. Ho, and Mike Chen, "A Fractional-N Digital MDLL with Background Two-Point DTC Calibration Achieving -60dBc Fractional Spur," in *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2021. **(Invited for demo)**

[12] Q. Zhang, **Shiyu Su**, J. Liu and Mike Chen, "CEPA: CNN-based Early Performance Assertion Scheme for Analog and Mixed-Signal Circuit Simulation," in *2020 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2020.

[13] J. Liu, M. Hassanpourghadi, Q. Zhang, **Shiyu Su** and Mike Chen, "Transfer Learning with Bayesian Optimization-Aided Sampling for Efficient AMS Circuit Modeling," in *2020 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2020.

Ph.D. (2013-2019):

[14] **Shiyu Su** and Mike Chen, "A SAW-Less Direct-Digital RF Modulator with Tri-Level Time-Approximation Filter and Reconfigurable Dual-Band Delta-Sigma Modulation," in *IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers*, Feb. 2020.

[15] **Shiyu Su**, "Digital to radio frequency conversion techniques," *Ph.D. dissertation*, 2019.

[16] **Shiyu Su** and Mike Chen, "A 1–5GHz Direct-Digital RF Modulator with an Embedded Time-Approximation Filter Achieving -43dB EVM at 1024 QAM," in *IEEE Symp. on VLSI Circuits Dig. Tech. Papers*, C20-C21, Jun. 2019.

[17] M. Hassanpourghadi, Q. Zhang, P. Sharma, J. Nam, **Shiyu Su**, S. Chowdhury, J. Sathyamoorthy, W. Unglaub, F. Wang, Mike Chen, Sandeep Gupta, Anthony Levi, W. Hansford and W. Taylor, "Automated Analog Mixed Signal IP Generator for CMOS Technologies," *GOMACTech '19*, March 2019.

[18] **Shiyu Su** and Mike Chen, "A 16-bit 12GS/s Single/Dual-Rate DAC with a Successive Bandpass Delta-Sigma Modulator Achieving <-67dBc IM3 within DC to 6GHz Tunable Passbands," *IEEE J. Solid-State Circuits (JSSC)*, Dec. 2018. **(Invited)**

[19] **Shiyu Su** and Mike Chen, "A 16-bit 12GS/s Single/Dual-Rate DAC with Successive Bandpass Delta-Sigma Modulator Achieving <-67dBc IM3 within DC to 6GHz Tunable Passbands," in *IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers*, Feb. 2018. **(Invited for demo)**

[20] **Shiyu Su** and Mike Chen, "A 12-Bit 2 GS/s Dual-Rate Hybrid DAC with Pulse-Error Pre-Distortion and In-Band Noise Cancellation Achieving > 74 dBc SFDR and <−80 dBc IM3 up to 1 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits (JSSC)*, vol. 51, no. 12, pp. 2963–2978, Dec. 2016. **(Invited)**

[21] **Shiyu Su** and Mike Chen, "A 12b 2GS/s Dual-Rate Hybrid DAC with Pulsed Timing-Error Pre-Distortion and In-Band Noise Cancellation Achieving >74dBc SFDR up to 1GHz in 65nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers*, pp. 456–457, Feb. 2016.

[22] **Shiyu Su**, Tu-I Tsai, Praveen Kumar Sharma and Mike Chen, "A 12 bit 1GS/s Dual-rate Hybrid DAC with an 8GS/s Unrolled Pipeline Delta-Sigma Modulator Achieving > 75 dB SFDR over the Nyquist Band," *IEEE J. Solid-State Circuits (JSSC)*, vol. 50, no. 4, pp. 896–907, Apr. 2015. **(Invited)**

[23] **Shiyu Su**, Tu-I Tsai, Praveen Kumar Sharma and Mike Chen, "A 12-bit Hybrid DAC with 8GS/s Unrolled Pipeline Delta-Sigma Modulator Achieving >75dB SFDR over 500MHz in 65nm CMOS," in *IEEE Symp. on VLSI Circuits Dig. Tech. Papers*, pp. 1-2, Jun. 2014.

DETAILED RESEARCH EXPERIENCE

Micro-unmanned Aerial Vehicles (MAV) – Designer **2021-present**

- Implementing a bio-inspired hybrid (digital/analog/mixed-signal) computing flatform for MAV.
- Implementing a fast solver for LP/QP optimization problems demanded by advanced control algorithms (e.g., model predictive control with control barrier functions) using >7 bits memristor devices.
- Implementing energy/area-efficient peripheral circuits (data converters) for memristor-based computing.
- Implementing energy/area-efficient sensor fusion for high-precision control.

RF/Millimeter Wave Transceivers – Designer **2020-present**

- Implemented a >40-GHz multi-mode receiver front-end with a reconfigurable anti-aliasing filter.
- Implementing a 28-GHz power amplifier with efficiency enhancement at deep power backoff; applying a time-approximation filter in the combination of delta-sigma modulation for ultra-low in-band and out-of-band noise.

VCO-/Time-Based ADC – Designer **2019-present**

- Implementing a 12-bit 200MHz VCO-based sub-ranging ADC for low-power applications.
- Implemented an 8-bit 40GS/s time-based ADC with only eight time-interleaved channels and achieved the lowest FoM around the target regime.
- Explored reconfigurable signal transfer function for continuous-time delta-sigma ADC.
- Explored mostly digital ADC architectures that cover a wide range of specifications.

Low Power Injection-Locked Digital PLL – Designer **2018-present**

- Implemented a ring-based injection-locked digital PLL with ultra-low phase noise and spur in 65nm CMOS.
- A background two-point DTC calibration algorithm is used for precise injection locking in the PLL.
- A dithered TDC with adaptive comb-filter-assisted dither removal technique is used to ensure low-cost and accurate DTC error estimation.

Analog/Mixed-Signal Design Automation – Designer **2018-present**

- Explored low-cost learning algorithms for efficient synthesis of analog/mixed-signal (AMS) blocks such as operational amplifiers, data converters, and phase/delay lock loops.
- Explored circuit-topology-aware neural network structure for AMS circuit modeling and design.
- Explored a transfer learning algorithm with Bayesian optimization-aided sampling to significantly cut the required size of training datasets for neural network models.
- Applied CNN to extract circuit features from the transient waveform with much higher accuracy and speed than a human designer and used these features to expedite the prediction of circuit performance.

Direct Radio Frequency (RF) Transmitter – Designer **2018-present**

- Explored optimization algorithms for designing impulse response of a time-approximation filter.
- Implemented a sub-6GHz direct RF transmitter prototype in 65nm CMOS that supports multi-mode and multi-band applications (both FDD and TDD), including all previous 2G, 3G and 4G versions.
- Implemented a 0.5-5GHz direct RF transmitter prototype in 65nm CMOS with an embedded time-approximation filter achieving <-158dBc/Hz noise spectral density (NSD) and <-43dB EVM at 1024 QAM.

High-Speed and High-Resolution DAC (>GHz and >12bits) – Designer **2012-2018**

- Implemented a 16-bit 12GS/s prototype in 65nm CMOS that achieves < -167dBc/Hz in-band NSD and -85 to -67dBc IM3 up to Nyquist frequency with tunable bandpass DSM and iSinc-shaped pre-distortion.
- Implemented a 12-bit 2GS/s prototype in 65nm CMOS that achieves > 74dBc SFDR and < -80dBc IM3 up Nyquist frequency with in-band noise cancellation and pulsed error pre-distortion scheme.
- Implemented a 12-bit 1GS/s prototype in 65nm CMOS that achieves > 75dBc SFDR up to Nyquist frequency
- Implemented an 8-element 12-bit 500MS/s hybrid DAC array prototype for harmonic cancellation of a transmitter in 28nm CMOS with an interpolator-based image cancellation scheme.
- Implemented a 12-bit 500MS/s dual-rate hybrid DAC prototype for non-uniform ADC dithering signal synthesis in 28nm integrated with the ADC and digital dither removing processing module.

A 12-bit 1.6GS/s Interleaving SAR ADC in TSMC 65nm – Designer **2014**

- Designed a background comparator offset calibration loop for single-channel ADC.

Next Generation DSP-enable Phase Lock Loop (DPLL) in TSMC 65nm – Designer **2013**

- Implemented a background interference cancellation algorithm for a DPLL, including a CORDIC-based direct digital frequency synthesizer with >100dB SFDR and a gradient descent module.

ACADEMIC SERVICES

The IEEE Journal of Solid-State Circuits (JSSC) – Reviewer **2017-present**

The IEEE Solid-State Circuits Letters (SSC-L) – Reviewer **2018-present**

The IEEE Transactions on Circuits and Systems I (TCAS-I) – Reviewer **2015-present**

The IEEE Transactions on Circuits and Systems II (TCAS-II) – Reviewer **2014-present**

The IEEE Transactions on Microwave Theory and Techniques (TMTT) – Reviewer **2021-present**

The IEEE Transactions on Very Large-Scale Integrated Systems (TVLSI) – Reviewer **2016-present**

The IEEE Sensor Journal – Reviewer **2021-present**

The IEEE Open Journal of Circuits and Systems (OJCAS) – Reviewer **2021-present**

The IEEE Transactions on Circuits and Systems for Video Technology (TCSVT) – Reviewer **2017-present**

The IEEE International Symposium on Circuits and Systems (ISCAS) – Reviewer **2017-present**

Tenth Research Festival, Ming Hsieh Institute, USC – Organizer **2019-2020**

Integrated Systems Seminar Series, Ming Hsieh Institute, USC – Organizer **2017-2018**

SOCIETY MEMBERSHIP

Member of IEEE
Member of IEEE Circuits and Systems Society
Member of IEEE Solid-State Circuits Society

REFERENCES

Mike Shuo-Wei Chen
Email: swchen@usc.edu

Jan Westra
Email: jan.westra@broadcom.com

Keith Chugg
Email: chugg@usc.edu

Hossein Hashemi
Email: hosseinh@usc.edu

Sandeep Gupta
Email: sandeep@usc.edu

Jeffrey Sean Walling
Email: jeffrey.s.walling@utah.edu