

# Khaled Mohamed Hassan

**Email:** [khassan@usc.edu](mailto:khassan@usc.edu)

**Tel:** [Mobile] +(1) 424-217-9857

**Address:** 1219 West 27<sup>th</sup> street, Los Angeles, California, USA.

---

## Education

---

- **Ph.D.** in Electrophysics, USC(University-of-Southern-California) (Spring 2022 ~ Spring 2027) (**Excepted**).
- **M.Sc.** in Electronics and Communications Engineering, Ain-Shams University (**November 2019**).  
**Thesis entitled by:** “Charge-Steering Circuits for Low-Power Applications” (**GPA: 3.6/4**).
  - The thesis aimed to study the design of charge-steering circuits for different applications.**Advisors: Prof. Emad Hegazi and Dr. Sameh Ibrahim.**  
**M.Sc. Curriculum Emphasis:** Advanced Analog, Power Management, RF Circuits and Systems, High-Speed Serial Links, and Digital IC.
- **B.Sc.** in Electronics and Communications Engineering, Ain-Shams University (**July 2013**).  
**Cumulative Grade: Distinction with honor (Ranked: 7<sup>th</sup>/160).**  
**Graduation Project:** “Sub-1GHz Transceiver for IoT Applications” sponsored by Silicon-Vision. Responsible to design a **power amplifier** plus PLL system integration.

---

## Research AND Professional Interests

---

Power Management, RFICs, IoT, mmWaves, Wireline Transceivers, PLLs and Data Converters.

---

## Publications

---

### Papers

- [1] K. M. Hassan and S. A. Ibrahim, "Charge-Steering Flip-Flop for Ultra-High-Speed Wireline Applications," *2019 36th National Radio Science Conference (NRSC)*.
- [2] K. M. Hassan and S. A. Ibrahim, "A Non-Return-to-Zero Charge-Steering Flip-Flop for High-Speed Wireline Transceivers," *2019 IEEE Jordan International Joint Conference on Electrical Engineering and Information Technology (JEEIT)*.
- [3] M. A. Saif, K. M. Hassan, A. Abdelati and S. A. Ibrahim, "A 34-fJ/bit 20-Gb/s 1/8-rate Charge-Steering DFE for IoT Applications," *2019 17th IEEE International New Circuits and Systems Conference (NEWCAS)*.
- [4] M. A. Saif, A. T. Kotb, K. M. Hassan and S. A. Ibrahim, "A 112-fJ/bit 10-Gb/s Charge-Steering Equalizer Utilizing a Discrete-Time Linear Equalizer," *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*.
- [5] M. A. Saif, K. M. Hassan and S. A. Ibrahim, "A 20-Gb/s Charge-Steering Equalizer Utilizing Highly-Efficient Charge-Steering Linear Equalizer," *Microelectronic Journal 2020 (MEJ)*. [To be published soon].

### Patents

- [1] High accuracy current sensing of switched capacitor DC-DC converters [In the filing process].
  - [2] An adaptive highly efficient startup circuitry employing a supply tracking mechanism [In the filing process].
  - [3] Highly efficient supply-referred rail generation using switched capacitor DCDC Converter [In the filing process].
- 

## Work Experience

---

- Senior Staff Analog Design Engineer at [Vidatronic, Inc.](#) (Jan 2021 – Dec 2021)
  - Staff Analog Design Engineer at [Vidatronic, Inc.](#) (Sep 2018 – Jan 2021)
- Founded by Prof. Edgar Sanchez-Sinencio from Texas A&M.

- **Responsibility**
  - **Top-level system design.**
  - Designed challenging blocks.
  - **Leading Analog/RF design activities.**
  - Support/Monitor the design team members and help them to reach a good design.
  - Create/Update the chip hierarchy and the **top-level schematics.**
  - Manage the **communication** with the other activities within the project (**digital/layout/PCB design**).
  - Contribute to the planning for the **verification and testing.**
- **Senior Analog/RFIC Design Engineer** at [Si-Vision LLC](#). (Feb 2017– Sep 2018)  
Working exclusively for **Synopsys, Inc. since wireless IPs Assets’ acquisition at July 2015.**
- Analog IC Design Engineer at [Si-Vision LLC](#). (Nov 2013 – Feb 2017)
  - **Responsibility**
    - **RX system design** where each block specification was defined to meet the system requirements of sensitivity, linearity and current consumption targets
    - **Designing of matching networks, PA, LNA, Mixer, VGA, complex-filter, tuners and limiters.**
    - **EM simulation for the entire RF chain.**
    - PCB design for the RF path.
    - Owner of the **top-level chip verification.**
    - Testing and measurement including **qualification testing** for the BLE.

## Honors AND Awards

1. Nominated for the best M. Sc. thesis in 2019.
2. Peer reviewer at IEEE CAS society (2019 – Present).
3. Best employee in Silicon-Vision in 2015.

## Languages AND Skills

### Key Skills:

- |                                             |                                     |
|---------------------------------------------|-------------------------------------|
| ○ Analog Circuit Design                     | ○ SERDES/PLL/DLL/VCO                |
| ○ RF/Mixed Signal Design                    | ○ Switch Capacitor                  |
| ○ Fin-FET Experience                        | ○ Amplifiers/Comparators            |
| ○ High Speed RF Transceiver Design          | ○ Process evaluation and monitoring |
| ○ Voltage Regulators/References             | ○ Low voltage and low power design  |
| ○ Matching networks (Internal and External) | ○ SoC Integration                   |
| ○ LNA and Mixers                            | ○ Converters (A2D, D2A)             |
| ○ Complex Filter and Limiters               | ○ DCDC converters                   |

### Hand-on experience with Lab instruments and measurements.

- Network analyzer, spectrum analyzer, oven, testing boards, ... and signal generators.

### Design Tools:

- Analog/Mixed-signal Tools: Synopsys, Mentor and Cadence (Virtuoso ADE, Spectre, Hspice, OCEAN scripting, Custom Designer, SAE, Eldo, Assura, QRC, Calibre).
- EM Simulators: Sonnet, HFSS, ADS and Helic (RaptorX and VeloceRF).
- Digital Simulators: Model-Sim, SimVision, VCS, Nano-sim, Silicon-Smart.
- Mathematics Tools: Matlab and Scilab.

**Programming Languages:** Verilog-AMS, Verilog and VHDL.