Subhajit Dutta Chowdhury

https://www.linkedin.com/in/subhajit-dutta-chowdhury-3aba7992/

Email : duttacho@usc.edu
Mobile : +1-213-713-8280

EDUCATION

- **University of Southern California** — Los Angeles, CA
  PhD in Electrical and Computer Engineering — *August 2017 – present*
  VLSI System Design, Applied Cryptography, Computer Systems Organization, Design for Testability, Mathematical Model for Cyber-physical System Design, Mixed Signal Integrated Circuit Design, Machine Learning, Graph Signal Processing

- **Institute of Engineering and Management** — Kolkata, India
  B.Tech in Electronics and Communication Engineering — *August 2012 – May 2016*
  Data Structures and Algorithms, Microelectronics and VLSI design, Digital Electronics and Integrated Circuits, Analog Electronics Circuits, Circuit Theory and Networks, Solid State Devices, Microprocessors and Microcontrollers

EXPERIENCE

- **Google** — Sunnyvale, CA
  Research Hardware Engineering Intern (CI2) — *May. 2022 - Aug. 2022*

  Defect Oriented Fault Model ATPG for improving Silicon Quality
  - Establishing the flow for generating cell-aware fault models of standard library cells in advanced technology node.
  - Analyzing the impact of introducing advanced fault models on improving the fault coverage compared to traditional fault models for chip designs.
  - Advanced fault modeling helps in capturing more manufacturing defects and address silent data corruption issues.

- **University of Southern California** — Los Angeles, CA
  Ph.D. Graduate Student (Advisor: Prof. Pierluigi Nuzzo) — *Aug. 2019 - Present*

  Circuit reverse engineering using deep learning
  - Developed a Graph Neural Network (GNN) based technique for identification of control registers in a design to enable control logic reverse engineering.
  - Created graph dataset by synthesizing RTL designs of different benchmarks ranging from cryptographic cores to logic blocks of microprocessor.
  - Explored extensively how different types of GNN models performed in the identification of the control registers.
  - Working on enhancing the current framework for analyzing the security vulnerabilities of sequential logic locking techniques.

  Analysis of information leakage from structural signatures of different combinational logic locking techniques
  - Currently working on devising a new learning based logic locking attack technique that leverages GNNs to analyze the information leakage from the structural signatures of different logic locking techniques to attack them.
  - Comparing the effectiveness of different deep learning models like MLPs, CNNs, and GNNs in attacking the exisitngs logic locking techniques
  - Simultaneously working on devising new logic locking techniques that can reduce information leakage from their structural signatures.

  Analysis of reconfigurable-logic-based circuit locking techniques
  - Developed an efficient logic locking technique that uses circuit testability measures to find the optimal location for insertion of reconfigurable logic and routing blocks.
  - Analyzed the Boolean Satisfiability (SAT) based attack resiliency and design overhead of existing and proposed reconfigurable-logic-based locking techniques.

  Teaching Assistant
  - Responsible for holding discussion sessions and grading mid-terms, finals, and final projects for MOS VLSI Design (EE 477L), and VLSI System Design (EE577A) in fall 2019 and spring 2020 respectively.

- **University of Southern California** — Los Angeles, CA
  Ph.D. Graduate Student (Advisor: Prof. Mike Chen) — *Aug. 2017 - Aug. 2019*

  Machine learning based analog mixed-signal circuit generator
  - Modelled different circuit blocks like single stage amplifier, sample and hold, and phase comparator with neural networks and open sourced them. https://github.com/USCPOSH/AMPSE

- Used these models to generate complete designs of SAR-ADC and Delay Locked Loop (DLL) with wide design specification range with minimum human designer intervention in the loop.

- **Bose Institute** Kolkata, India
  Undergraduate Researcher; Advisor: Dr. Suman Banik *Dec 2015 - May 2016*
  Electronic Circuit Representation of Genetic Regulatory Networks
  - Designed and validated electronic circuits to mimic genetic regulatory networks namely repressilator, and genetic toggle switch.

SELECTED PUBLICATIONS

1. **S. Dutta Chowdhury**, K. Yang, P. Nuzzo, "ReIGNN: State Register Identification Using Graph Neural Networks for Circuit Reverse Engineering," *accepted to International Conference on Computer Aided Design (ICCAD) 2021.*
2. **S. Dutta Chowdhury**, G. Zhang, Y. Hu, P. Nuzzo "Enhancing SAT-Attack Resiliency and Cost-Effectiveness of Reconfigurable-Logic-Based Circuit Obfuscation," *International Symposium on Circuits and Systems (ISCAS) 2021.*
3. **S. Dutta Chowdhury**, K. Yang, P. Nuzzo "ReIGNN+: State Register Identification Using Graph Neural Networks for Circuit Reverse Engineering," *journal under review.*
4. **S. Dutta Chowdhury**, Z. Wang, Y. Hu, K. Yang, P. Nuzzo "GLean: Graph Learning-Driven Structural-Functional Attack to Logic Locking," *under review.*
5. Y. Hu, K. Yang, **S. Dutta Chowdhury**, P. Nuzzo, "Risk-Aware Cost-Effective Design Methodology for Integrated Circuit Locking," *Design Automation and Testing in Europe (DATE) 2021.*
6. M. Hassanpourghadi. et. al, "Automated Analog Mixed Signal IP Generator for CMOS Technologies," *GOMACTECH 2019.*
7. R. Chakraborty, **S. Dutta Chowdhury**, A.K. Chakraborty, "Talbot self-imaging phenomenon under Bessel beam illumination," *Applied Physics B.*
8. M. Sarkar, R. Roy Chaudhuri, **S. Dutta Chowdhury**, N. Kumar Thakur, S. Chowdhury, "Onset of Chaos for Different Non Linear Systems by Varying System Parameters," *Advances in Optical Science and Engineering, Springer Proceedings in Physics.*
9. Y. Hu, **S. Dutta Chowdhury**, k. Yang, M. Munir, J. Bollareddy, P. Nuzzo "DECOR: Enhancing Logic Locking Against Machine Learning-Based Attacks," *under review.*

COURSE PROJECTS

- **VLSI Design Mini Project**: Design of a General Purpose 5-stage Pipelined Microprocessor with Software and Hardware Components in Cadence. Nov 2018 - Dec 2018
- **Mixed Signal Integrated Circuit Design Mini Project**: Design of a Single Stage Fully Differential Operational Transconductance Amplifier (OTA) Nov 2018 - Dec 2018
- **Mixed Signal Integrated Circuit Design Mini Project**: Design of a 8-bit,1GS/s Time-Interleaved SAR ADC in 45nm CMOS Technology. March 2019 - May 2019
- **Design for Testability Mini Project**: Implementation of ATPG algorithm (PODEM) and Fault Simulator for some ISCAS'85 benchmark circuits. Nov 2019 - Dec 2019
- **Designing a recommendation system for HM personalized fashion recommendations**: Designing a recommendation system for H&M personalized fashion recommendations for existing and new customers. April 2022 - May 2022
- **Analyzing Adversarial Attacks on Graphs**: Analyzed the impact of different types of adversarial attacks on the graph Fourier spectrum April 2022 - May 2022

SERVICES

- **High School Student Mentoring**: Mentored 4 high school students in the summer of 2018 and 2021 through the USC Viterbi Summer High School Intensive in Next-Generation Engineering (SHINE) program.
- **Reviewer**: Reviewer for DAC(2019, 2020, 2021), DATE(2019, 2020, 2022), TCAD
- **President, IEM SPIE-OSA Student Chapter**: Conducted educational outreach programs in underprivileged communities. Represented my undergrad university at the SPIE Optics and Photonics Conference in 2015.

TECHNICAL SKILLS

- **Programming Languages**: Python, Java, C++ **Simulation Environments**: Cadence (Virtuoso), Synopsys (VCS, Design Compiler, Tetramax), MATLAB, Modelsim **HDLs**: Verilog. **ML Tools**: Pytorch

AWARDS

- **2021 DAC Young Fellow**: Awarded the DAC young fellowship to attend DAC 2021
- **2015 SPIE Officer Travel Grant**: Awarded SPIE Officer Travel Grant to represent the Student Chapter at Optics+Photonics 2015, San Diego, CA