UNIVERSITY OF SOUTHERN CALIFORNIA

COMPUTER ENGINEERING

SCREENING EXAMINATION

EE 552

Asynchronous VLSI Design

SUGGESTED READING

Book: P. A. Beerel, R. O. Ozdag, M. Ferretti, A Designer's Guide to Asynchronous VLSI, Cambridge University Press, 2010, ISBN13 9780521872447

Papers:
1. "Loihi: A Neuromorphic Manycore Processor with On-Chip Learning," M. Davies et. al., IEEE Micro, 2018.
2. "Metastability and Synchronizers: A Tutorial", R. Ginosar, IEEE Design & Test, Sept/Oct. 2011.
3. D. Hand et al., "Blade -- A Timing Violation Resilient Asynchronous Template," 2015 21st IEEE International Symposium on Asynchronous Circuits and Systems, Mountain View, CA, USA, 2015, pp. 21-28, doi: 10.1109/ASYNC.2015.13.
4. "SERAD: Soft Error Resilient Asynchronous Design Using a Bundled Data Protocol," S. Aketi et. al, IEEE TCAS, May, 2020.

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Please be aware that these references are for guidance in BASIC knowledge. Ph.D. candidates are screened on the basis of talent, course knowledge, independent reading and experience.

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