Kyle Marino

108 Whits Road ▪ Mountain View, California 94040
650.946.7854 kmarino@usc.edu

Qualification Summary

Graduate electrical computer engineering student pursuing a Master's at the University of Southern California. Experienced in machine-learning, FPGA design, embedded software, cloud computing, and board design.

Education

USC Viterbi School of Engineering ■ Los Angeles, CA **May 2024**

BS Electrical and Computer Engineering (2023) - Presidential Scholarship, Graduated Summa Cum Laude
MS Computer Engineering (2024)
Coursework: Computer Systems Organization, SOC Design, Internet and Cloud Computing, Computational Intelligence and Neural Learning, Deep Learning, Probability Theory, Linear Algebra

Experience

Directed Research ■ Los Angeles, CA **Feb 2023 – Present**

Research under Dr. Viktor K. Prasanna

- Designed a Vision Transformer accelerator on FPGA, achieving up to a 17.89x reduction in memory bandwidth and a 2.16x improvement in throughput per DSP over SOTA designs
- Marino et al. "ME-ViT: A Single-Load Memory-Efficient FPGA Accelerator for Vision Transformers." (To be published)

AMD/Xilinx ■ San Jose, CA **May 2023 – Aug 2023**

RTL Integration Intern

- Developed scripts for generating interposer layers to connect various FPGA dies within one package
- Designed a large-scale distributed RTL design rule verification system that analyzes full-chip RTL

AMD/Xilinx ■ San Jose, CA **May 2022 – Aug 2022**

SOC Integration Intern

- Ran full-chip builds of FPGAs and completed EMIR simulation with Red Hawk SeaScape
- Worked with various teams to create a set of Python tools for automatic EMIR report generation
- Implemented a custom build flow process in Perl to automate simulation and integrated with Python toolset

USC Coursework ■ Los Angeles, CA **Aug 2022 – Present**

EE 542 (Internet and Cloud Computing) Class Projects

- Designed a custom file transport protocol with multithreaded UDP sockets that outperforms TCP over a network with 20% loss, achieving over 75 Mbps out of 80 Mbps theoretical
- Modified TCP in the Linux kernel to improve throughput over a link with 20% loss, increasing throughput from 480 Kbps to 10 Mbps

USC Rocket Propulsion Laboratory ■ Los Angeles, CA **Sep 2019 – Jan 2022**

Lead FPGA Design Engineer For a Custom IMU system

- Architect and Designer for a 4 sensor data collection and processing system using the Intel MAX10 FPGA
- Designed a custom float processing ALU for real-time quaternion integration of high throughput data.
- Developed Python compiler to generate ROM-based instructions for the processing unit.

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- Simulated and Verified Python compiler and processing unit logic using ModelSim
- Designed Custom Verilog RTL for implementation of the SD Bus, I2C, and SPI interfaces for an ADC, Gyroscope, Magnetometer, and Accelerometer devices.

PCB Designer for a Battery Management Board

- Responsible for the Design and Construction of a new battery management PCB for the Rocket Avionics system.
- Implemented battery protection, monitoring, and charging features.
- Developed a C++ driver to interface with the state-of-charge IC.
- Ran battery tests for capacity and performance characteristics.
- Hands-on lab bring-up and debugging using test equipment.

Really, Inc. ■ Mountain View, CA **Jun 2018 – Dec 2018**

Backend Development Intern

- Collaborated with a small team to develop a machine-learning engine that analyzes changes in social media posts to detect the early onset of potential neurodegenerative diseases.
- Developed a program with Node.js and Java that analyzes and stores linguistic changes over time.

Project ■ Mountain View, CA **Dec 2016 – Jun 2018**

Quadcopter Design

- Designed and built a fully functioning, self-stabilizing quadcopter with a camera and remote-control capabilities.
- Engineered all embedded software, including the drivers for various sensors and serial communication

Leadership

Los Altos High School ■ Los Altos, CA **Jan 2017 – Jun 2019**

Los Altos Hacks

- Contacted companies for scholarships and helped the team raise over $25,000 for the event
- Worked with a team of 12 students to secure funding, a venue, judges, and participants for the hackathon
- Mentored hackathon participants and improved their programming and web design skills.

Boy Scouts of America ■ Los Altos, CA **Jun 2006 – Sep 2018**

Eagle Scout

- Leader for the restoration of tables and benches at the Los Altos History Museum (Eagle Scout project).
- Organized weekly meetings, planned camping trips, and was an Assistant Patrol Leader for younger Boy Scouts.

Technical Skills

- ✓ FPGA Development
- ✓ Verilog RTL Design
- ✓ SPI, I2C, and SD Bus Interfaces
- ✓ IMU, Accelerometer, and Gyro
- ✓ PCB Design in Altium
- ✓ Vitis HLS Development
- ✓ C++ Driver Development
- ✓ Python and Matlab
- ✓ AWS, Spark, Hadoop, MPI