REZWAN A RASUL

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EDUCATION

University of Southern California Present
PhD in Electrical and Electronics Engineering
CGPA: 3.76/4.00
Research focus: Energy-efficient neural network accelerator design using analog & mixed-signal integrated circuits.

Tokyo Institute of Technology March 2016
MEng in Physical Electronics
CGPA: 2.87/3.00
Thesis: Designed and laid out two 12-bit, 10MSps, 0-5V differential input synchronous SAR ADCs for automotive sensor application.

Tokyo Institute of Technology March 2014
BEng in Electrical and Electronics Engineering
CGPA: 2.91/3.00 (ranked 2nd out of 100)
Thesis: Simulated and analyzed LDO regulator as a power control circuit in SAR ADC.

SKILLS

- Design Tools: Cadence Virtuoso Suite (Schematic Editor, Layout Editor, Analog Design Environment, Spectre), AFS, SPICE, Verilog-A, Allegro
- Core Competencies: In-memory computing chip tapeout (algorithm, schematic, layout design) and measurement, Training-inference-quantization of neural network and mapping to IC, Analog-to-Digital converter design, Development of circuit design automation tool and measurement automation script
- Design technology node: 65nm CMOS, 16nm and 12nm FinFET
- Programming language: Python (TensorFlow, NumPy, SciPy), MATLAB, C
- Operating system: Windows and Linux (Red Hat)
- Natural language: English (Fluent), Bengali (Native), Japanese (Intermediate, N1)

PUBLICATIONS

- R. A. Rasul, MSW Chen, "A 128x128 SRAM Macro with Embedded Matrix-Vector Multiplication Exploiting Passive Gain via MOS Capacitor for Machine Learning Application," *IEEE CICC*, April 2021
- R. A. Rasul, P. Teimouri and M. S.-W. Chen, "A time multiplexed network architecture for large-scale neuromorphic computing," *IEEE MWSCAS*, August 2017
- M Hassanpourghadi, R. A. Rasul, MSW Chen, "A Module-Linking Graph Assisted Hybrid Optimization Framework for Custom Analog and Mixed-Signal Circuit Parameter Synthesis," *ACM TODAES*, September 2021
- M. Hassanpourghadi, S. Su, R. A. Rasul, et al., "Circuit Connectivity Inspired Neural Network for Analog Mixed-Signal Functional Modeling," *ACM/IEEE DAC,* December 2021

ACADEMIC PROJECTS

- A differential amplifier design for switched capacitor multiplying DAC stage
  Performed circuit analysis and applied gm/ID method for design.
- A general-purpose 5-stage microprocessor design
  Python coding of instruction fetch and decoding stage. Schematic design of register file (DFF), cache memory (SRAM), and arithmetic logic unit including 8b multiplier, 16b adder, etc.
- A wideband LNA, harmonic reject quadrature mixer and a differential VCO design
  Derived theoretical value of noise figure, IIP3, S11, and conversion gain and compared with the SPICE simulation.

WORK EXPERIENCE

Research Assistant

- RA of Analog Mixed Signal IC group at USC (Prof. Mike Chen) August 2016 – Present
  Led the neural network accelerator project as the only student designer.
  Engaged in the CAD tool development project by doing simulation, codebase development, and debugging.
  Involved in sensor fusion circuit design for the micro-aerial vehicle project.
- RA of Okada laboratory at Tokyo Tech (Prof. Akira Matsuzawa) April 2013 – September 2013
  Performed design space exploration and layout of interpolated pipeline ADC.

Teaching Assistant and Mentoring

- TA of EE 582, EE 348L at USC — Fall 2022, Fall 2018
  Instructed PCB design labs, designed NN accelerator project, and grading.
- Mentor of the SHINE program at USC — Summer 2020
  Guided a high-school senior to train and test a quantized neural network.
- TA of SAR ADC training session at Tokyo Tech — March 2015
  Trained participants to set up a testbench and perform ADC simulation using LTSpice.
- TA of EEE laboratory 3 (junior years undergrad course) at Tokyo Tech — October 2014 – February 2015
  Explained theory, assisted in VHDL coding, set up FPGA for distance measurement.

Internship

- **NEC Corporation**, IT Platform and Solution Division, Tokyo, Japan — Summer 2012
  Investigated security aspects of BitLocker encryption of Windows 7 OS.
  Examined the company's electronic information security policy and proposed amendments.
- **Sony Corporation**, Digital Imaging Division Tokyo, Japan — Summer 2012
  Measured performance of camera antennas in an antenna chamber at different frequencies.
  Compared performance of GPS- and GLONASS-compatible antennas.

HONORS AND AWARDS

- Electrical Engineering Academic Award for undergraduate merit position by IEEE, Japan — April 2014
- Monbukagakusho scholarship for undergraduate and master's program granted by MEXT, Japan — April 2009 - March 2016