10.1 A 10GS/s 8b 25fJ/c-s 2850um² Two-Step Time-Domain ADC Using Delay-Tracking Pipelined-SAR TDC with 500fs Time Step in 14nm CMOS Technology

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High-speed (>GS/s) medium-resolution ADCs are in high demand for wideband communication ICs. Meanwhile, the increasing cost in advanced technology nodes favors area-efficient ADC architectures. The traditional voltage-domain time-interleaved (TI) SAR ADC [1-2] is a popular choice for its superior power efficiency. However, its single-channel sample rate is generally limited to <1GS/s, necessitating a large number of TI channels in high-sample-rate scenarios. It inevitably increases implementation overhead, including capacitive loading to the input driver and total area consumption. Recently, time-domain ADCs [3-5] have shown promising sampling speed, but are mostly based on thermometer coded time-to-digital converters (TDC). Unfortunately, the circuit complexity for such Flash TDC grows exponentially with the target bit resolution. Existing SAR TDCs [6] demonstrate a lower complexity but are generally limited in sample rate (MS/s). In this work, we propose a two-step time-domain ADC that uses a first-stage Flash TDC with the residue time quantized by the second-stage SAR TDC, targeting the >GS/s regime. To further improve the throughput of SAR TDC conversion, we propose a delay-tracking pipelining technique that allows the SAR TDC to quantize two residue time samples, simultaneously. At the circuit level, we use a selective delay tuning (SDT) cell to provide the time reference required for SAR conversion without using an excessive number of delay stages. A proof-of-concept ADC prototype in 14nm CMOS technology with 2× time interleaving achieves 10GS/s with 37.2dB SNDR at Nyquist frequency. It measures an energy efficiency of 24.8fJ/conv-step and occupies an active area of 2850um², which are the highest reported energy efficiency and smallest area consumption among the state-of-the-art ADCs with >10GS/s [7].

One key design challenge for a high-speed time-domain ADC is a low-complexity TDC with fine LSB resolution. Figure 10.1.1 shows conventional TDCs with fine time resolution and the proposed SAR TDC using SDT cells. A time-domain ADC typically encodes the input voltage information into a time difference between two pulses (e.g., P_P and P_N in Fig. 10.1.1), and relies on the TDC for digitization. A traditional Vernier delay-line-based TDC uses the delay difference between two delay chains (τ_2-τ_1 in Fig. 10.1.1) for time quantization. It requires 2^{N+1} delay cells and 2^N time comparators for an N-bit conversion, imposing significant power and area overhead. Prior works on SAR TDCs [6] effectively reduce the number of time comparators; however, the time quantization step is still derived by selecting between two different delay chains using a multiplexer (MUX). Therefore, it still requires a large number of delay cells in addition to extra MUX delay. To alleviate this issue, we propose a SAR TDC architecture that dynamically changes the delay based on the time comparison result during bit trials, which is referred to as selective delay tuning. Whenever a bit trial reaches a decision, the SDT cell will insert an extra delay to either the positive or negative side of the TDC chain. The resulting delay difference will be used as the reference time for the successive approximation (SA) algorithm. Therefore, the proposed N-bit SAR TDC requires only $4\cdot(N\text{-}1)$ delay cells and N time comparators without a MUX, leading to lower noise and area/power consumption.

Figure 10.1.2 shows the proposed delay-tracking pipelined-SAR TDC and its timing diagram for the binary SA search. The SAR TDC is composed of five 1b stages, with each stage using a time comparator to perform a single bit trial, and an SDT cell to add or subtract a proper reference time. The operation mode of the time comparator is controlled by CLK. When CLK is LOW, the outputs will be reset to V_{DD}. When CLK is HIGH, the first rising edge of the two input pulses will trigger the comparator. Without pipelining, the same CLK signal is connected to all comparators, and it must remain HIGH until the input pulses completely propagate through the five conversion stages, thereby limiting the TDC throughput. Alternatively, applying a conventional TDC pipelining technique requires adding additional delay to the signal path to match the delay of each stage with the CLK period, which inevitably degrades the signal SNR or incurs significant power/area overhead to lower the added noise. To resolve this issue, we propose to insert delay (τ_{stage}) between the CLK signals for the 5-stage comparators (CLK<0:4> in Fig. 10.1.2), which does not degrade the signal SNR. The CLK delay should track with the propagation delay of the 1b stage (including the comparator and SDT delay), such that the CLK signal can return to LOW as soon as the input pulse propagates to the next 1b stage and the decision result is cached, thus increasing the throughput. As a result, two input pulses can be simultaneously processed by the SAR TDC. We refer to this implementation as a delay-tracking pipelined-SAR TDC, which helps double the throughput to reach 5GS/s.

Based on the delay-tracking pipelined SAR TDC architecture, we construct a two-step converter that performs the first 3 MSB conversions using a Flash TDC, and generates residue time signals (R_P and R_N) followed by the 5 LSB conversions via the SAR TDC, as shown in Fig. 10.1.3. The Flash TDC and residue time generation help reduce the maximum delay required for SDT cells in the SAR TDC, and hence allows us to optimize the jitter performance of the SDT cells. In order to linearly encode the sampled voltage information into the rising edge difference of two pseudo-differential pulses (P and N in Fig. 10.1.3), the sampled voltage needs to be ramped up and compared to a certain voltage threshold in the voltage-to-time conversion (VTC) block. Traditionally, the ramps are generated on both sampling capacitors via two separate charge pumps [3]. This ramp generation process is vulnerable to distortion, memory effect, and signal-dependent charge kickbacks. To improve the fidelity of VTC, we propose to create a common-mode ramp by charging a capacitor (C_{cm}) at the center node (V_c) of the sampling capacitors. After the VTC is completed, the C_{cm} will be reset to reduce memory effects and signal-dependent charge kickbacks to the input. Lastly, since our ramp generation only requires a single charge pump, it avoids the ramp slope mismatch issue that is seen in the conventional case.

The schematic of the SDT cell is illustrated in Fig. 10.1.3. We skew the relative strength between the pull-up and pull-down paths to create different falling-edge slopes at the intermediate node (*MID*). As a result, the transition time instant of the rising edge at the SDT cell output (*OUT*) is changed accordingly. This not only enables a fine time step (500fs in this design), but also yields less delay variation compared to Vernier delay cells due to much fewer transition edges. According to SPICE simulations, the standard deviation of the LSB time step variation is six times smaller than the Vernier TDC's counterpart, given the same transistor sizes in the unit delay cell.

Figure 10.1.4 shows the residue time generation and the first stage Flash TDC. The input pulses from the VTC block are first delayed by three coarse delay cells (each with a nominal delay of 16ps). Those delayed pulses are cross-compared with the input pulses via time comparators, which effectively create eight quantization levels, i.e., 3b Flash TDC. Afterwards, the residue time is generated by selecting the closest two rising edges between the input pulses and the coarse delayed pulses. Note that, the residue time range is re-adjusted from [0,16ps] to [-8ps, 8ps] by an SDT cell, to properly interface with the following-stage pseudo-differential SAR TDC operation.

The ADC is fabricated in 14nm CMOS with an active area of 2850um², as shown in Fig. 10.1.7. A foreground calibration is applied to tune the gain error between the first and second TDC stages. Figure 10.1.5 shows the measured SFDR and SNDR vs. input frequencies and the spectrum of the decimated ADC output for both single-channel and two-channel cases. The ADC shows <3dB SNDR variation across 0.1 to 5GHz input frequencies. The single ADC channel operating at 5GS/s achieves a 40.78dB SNDR and a 53.65dB SFDR at Nyquist, leading to a 16.6fJ/conv-step energy efficiency. The two-channel ADC operating at 10GS/s achieves a 37.24dB SNDR and a 50.67dB SFDR at Nyquist, leading to a 24.8fJ/conv-step energy efficiency. The performance comparison table is shown in Fig. 10.1.6. Compared with other state-of-the-art high-speed ADCs, this ADC achieves higher energy efficiency with the smallest active area.

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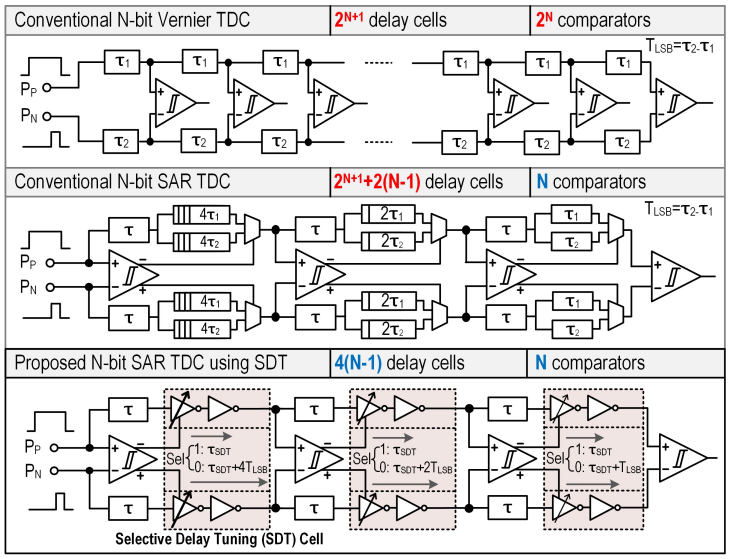

Figure 10.1.1: Conceptual diagram of the proposed SAR TDC using selective delay tuning (SDT) cell versus existing TDC architectures.

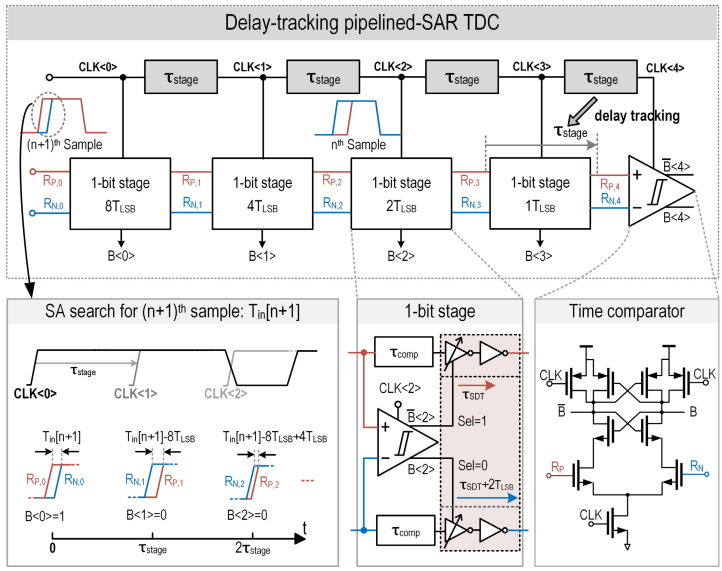

Figure 10.1.2: Proposed delay-tracking pipelined-SAR TDC and timing diagram.

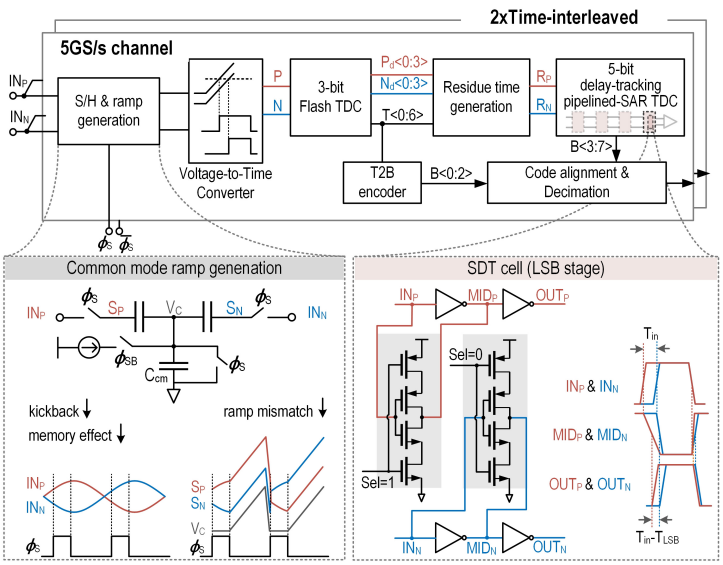

Figure 10.1.3: Block diagram of the two-step time-domain ADC and key building blocks.

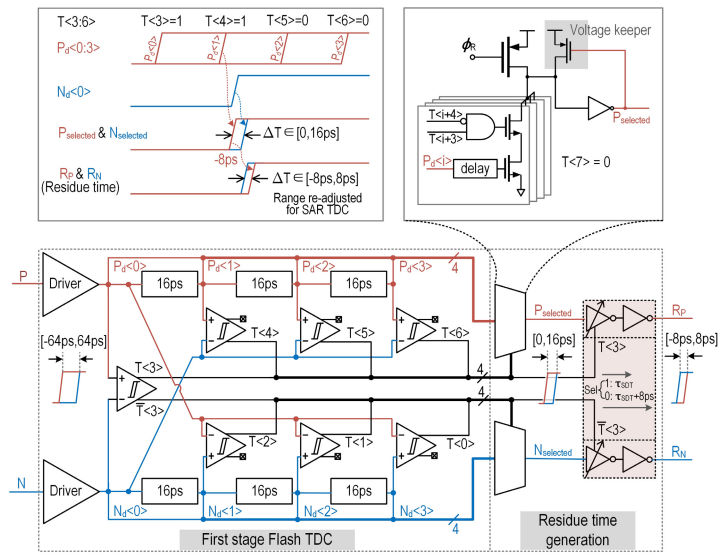

Figure 10.1.4: Implementation of the first-stage Flash TDC and the residue time generation.

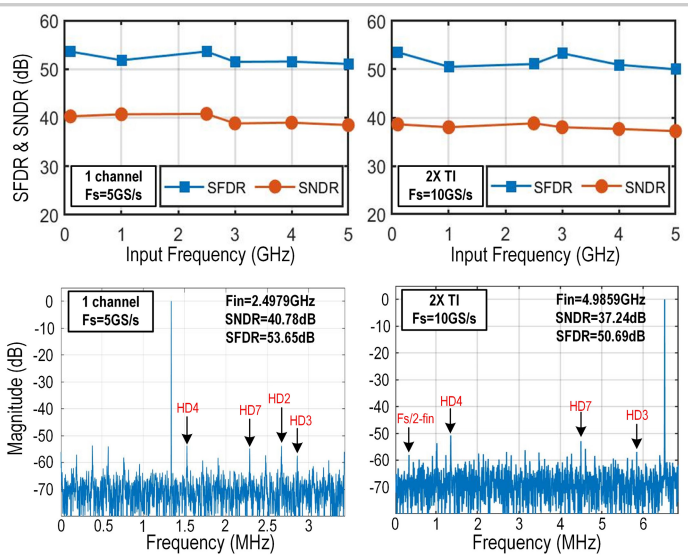

Figure 10.1.5: Measured SNDR/SFDR versus input frequencies and the spectrum of the decimated (by 729×) ADC output for a single channel and 2× time-interleaved (TI) channels.

	This work		ISSCC 20 M. Zhang[3]	CICC 19 M.Hassanpourghadi[4]	JSSC 19 D. Oh	JSSC 18 S. Zhu[5]	ISSCC 20 Z. Zheng	VLSI 19 M.Guo[1]
Architecture	Time-domain ADCs						Voltage-domain ADCs	
	Delay-tracking pipelined-SAR TDC		Interpolation TDC	Flash TDC	Interpolation TDC	Flash TDC	Dynamic Pipeline	TI-SAR
Technology	14nm CMOS		65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	28nm CMOS	28nm CMOS
Supply (V)	0.8		1	1	1	1	0.9	1
Resolution (bits)	8		8	7.3	6	8	6	10
# of TI channels	2	1	4	2	1	1	1	16
Sample rate (GS/s)	10	5	10	10	2.5	2	3.3	5
Power (mW)	14.8	7.4	50.8	29.7	7.5	21	5.5	29
SFDR@Nyq (dB)	50.69	53.12	52.8	40.7	45.07	48.36	45.5	59.6
SNDR@Nyq (dB)	37.2	40.8	40.1	32.5	33.84	40.68	34.2	48.5
FOM$_{Walden}$ @Nyq(fJ/conv-step)	24.8	16.6	61.5	86.0	74.7	119	40.0	26.7
Active area (um^2)	2850	1425	95000	15000	120000	80000	16600	103000

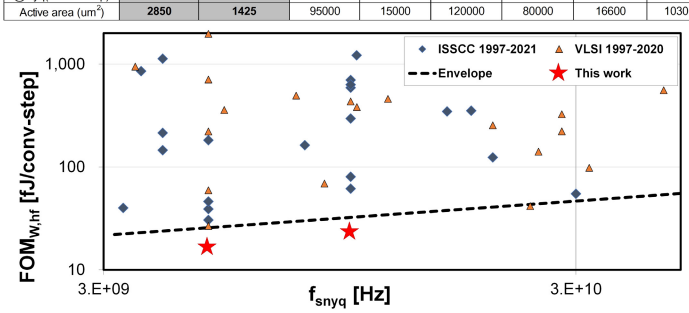

Figure 10.1.6: Performance summary and comparison with the state-of-the-art high-speed ADCs (>3GS/s).

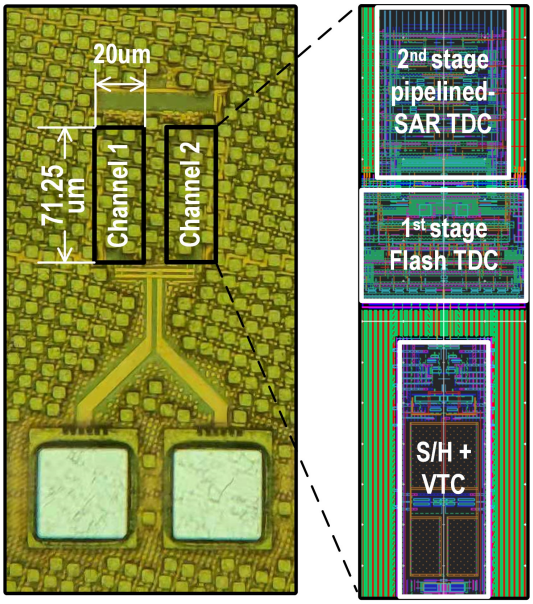

Figure 10.1.7: Die micrograph and layout of a single ADC channel.

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